

APN292

27 – 30 GHz

GaN Power Amplifier

PRODUCT DESCRIPTION

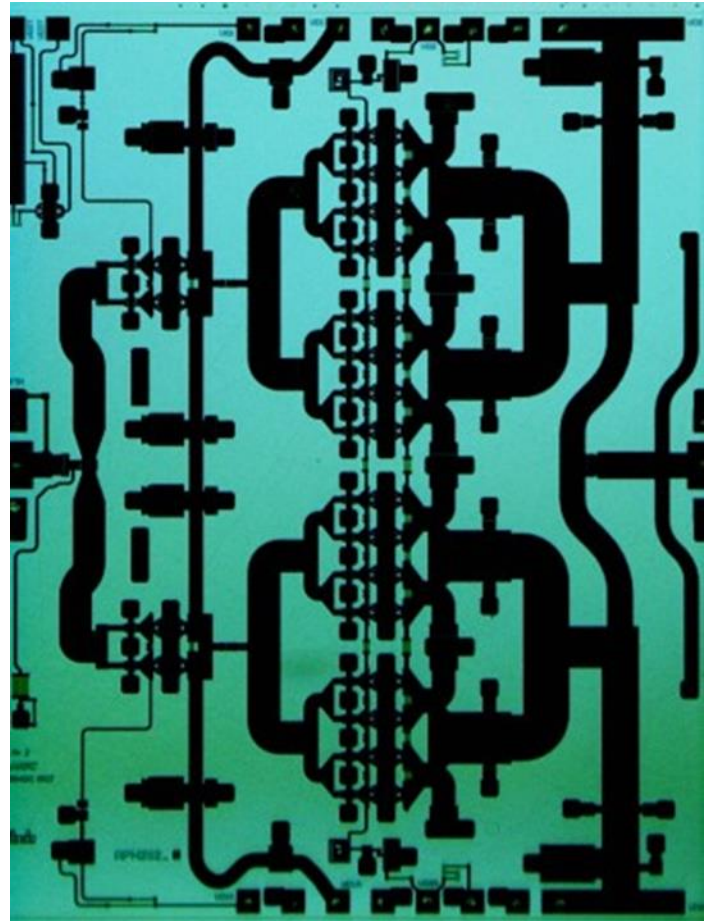
The APN292 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Ka-Band communication applications such as SatCom Terminals and point-to-point and point-to-multipoint digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

APPLICATIONS

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

PRODUCT FEATURES

- RF Frequency: 27 to 30 GHz
- Linear Gain: 20 dB typ.
- P_{sat}: ~16 W on wafer, pulsed
- P_{sat}: ~16 W in fixture, CW
- Die Size: 13.52 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 2.64 A



X=3.30 mm; y=4.10 mm

EXPORT INFORMATION

ECCN: 5A991.g

HTS (Schedule B) code: 8542.33.0001



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ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Drain Voltage	28	V
Gate Voltage Range	-8 to 0	V
Drain Current	4440	mA
Gate Current	4.32	mA
Power Dissipation*	92.4	W
Soldering Temperature	320	°C

*7W/mm of gate periphery

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Unit
Drain Voltage Range	20 - 26	V
Gate Voltage Range	-5 to -3	V
Stg 1 Drain Current (Idq)	500	mA
Stg 2 Drain Current (Idq)	500 – 2100	mA

ELECTRICAL SPECIFICATIONS

Parameter	Min	Typical	Max	Unit
Operational Frequency	27		30	GHz
Small Signal at 28V				
Small Signal Linear Gain	19	20	21	dB
Input Return Loss	-23.5		-3	dB
Output Return Loss	-15		-2	dB
On-Wafer Pulsed Power at 28V				
Psat (at 34 dBm)	45	46	46.5	dBm
Power Gain (at 34 dBm)	11	12	13	dB
PI _{db}	41.4	41.8	42.1	dBm
PAE (at 34 dBm)	21	23	26	%
Max PAE	26	28	32	%
Fixtured CW at 24V, 25°C Case Temp				
Psat (at 29 dBm)	42.7	43.3	43.7	dBm
Power Gain (at 29 dBm)	13.7	14.3	14.8	dB
PAE (at 29 dBm)	20	22	25	%
Max PAE	21	22	26	%
Drain Voltage		24		V
Stage 1 Gate Voltage		-4.027		V
Stage 2 Gate Voltage		-3.96		V
Stage 1 Idq		520		mA
Stage 2 Idq		2100		mA

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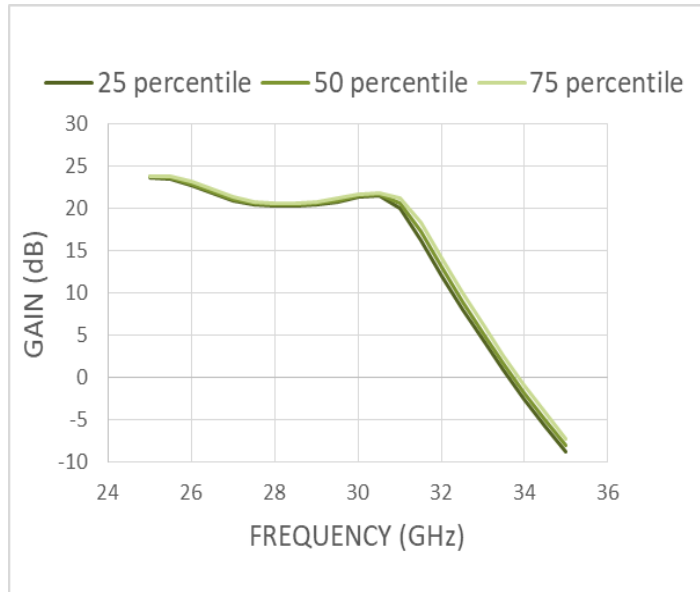
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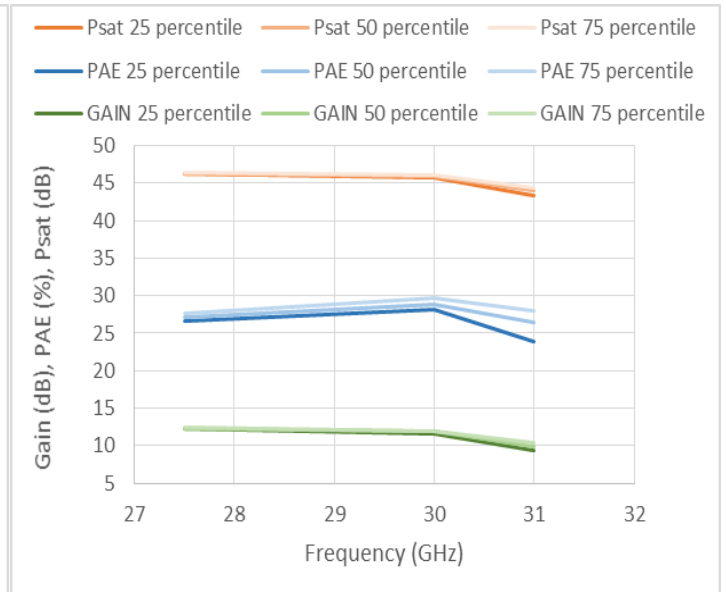
Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 28.0\text{ V}$, $I_{d1} + I_{d1a} = 520\text{ mA}$, $I_{d2} + I_{d2a} = 2100\text{ mA}$

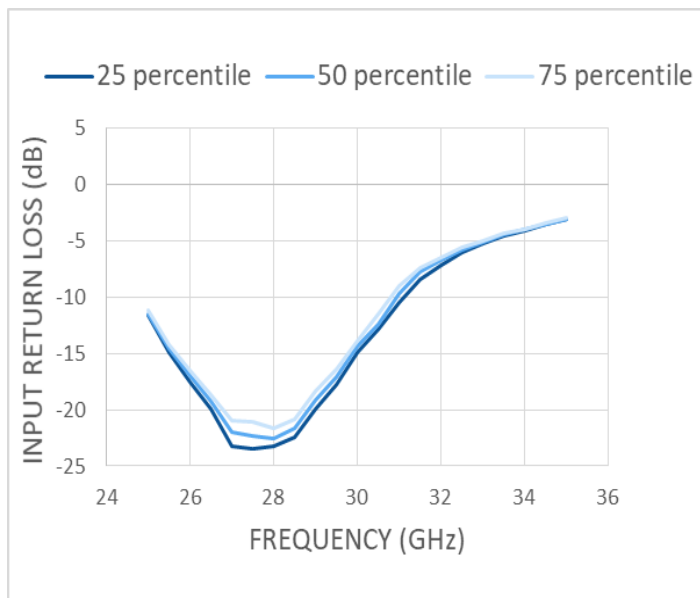
Small Signal Gain vs. Frequency



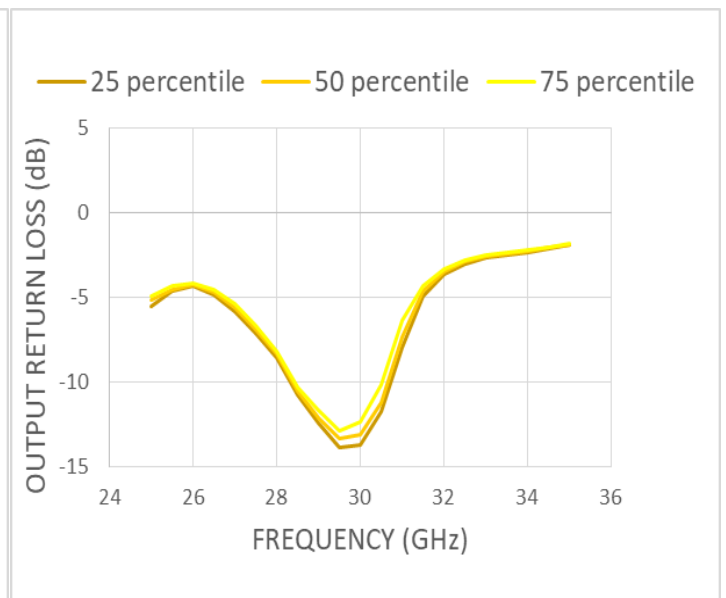
Large Signal PAE, Gain, PSAT vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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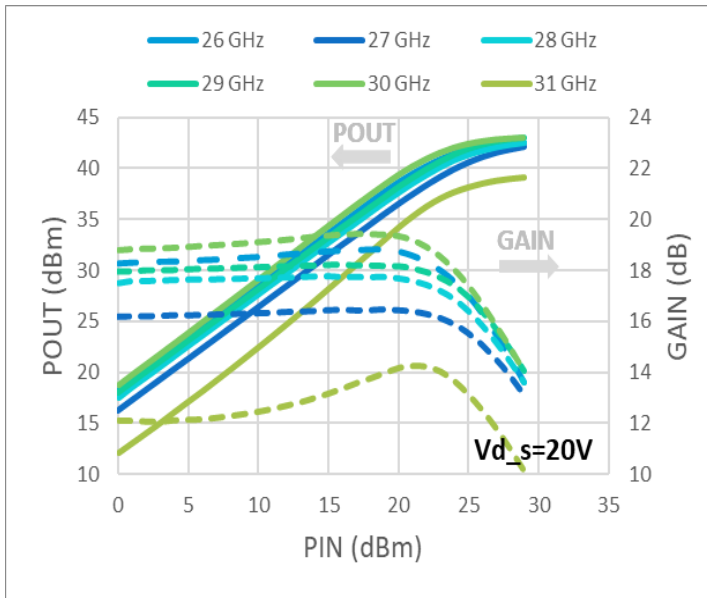
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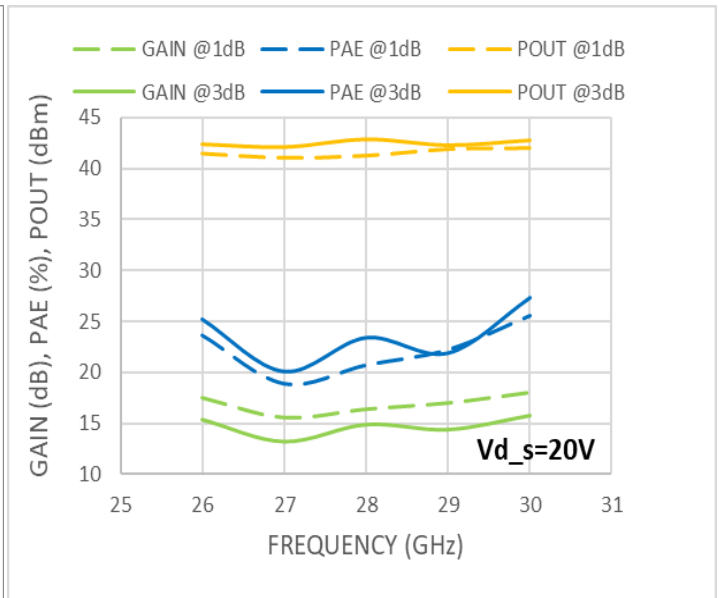
Fixture measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 20.0\text{ V}$, $I_{d1} + I_{d1a} = 520\text{ mA}$, $I_{d2} + I_{d2a} = 2100\text{ mA}$

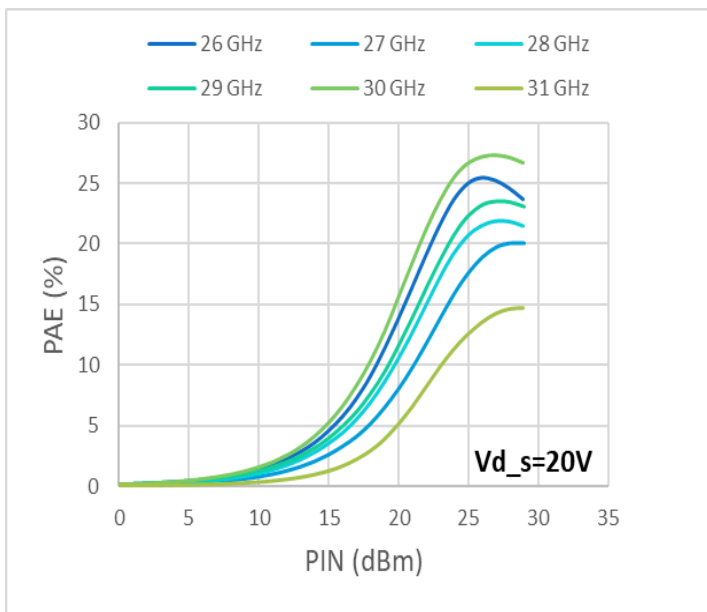
POUT and Gain vs. PIN



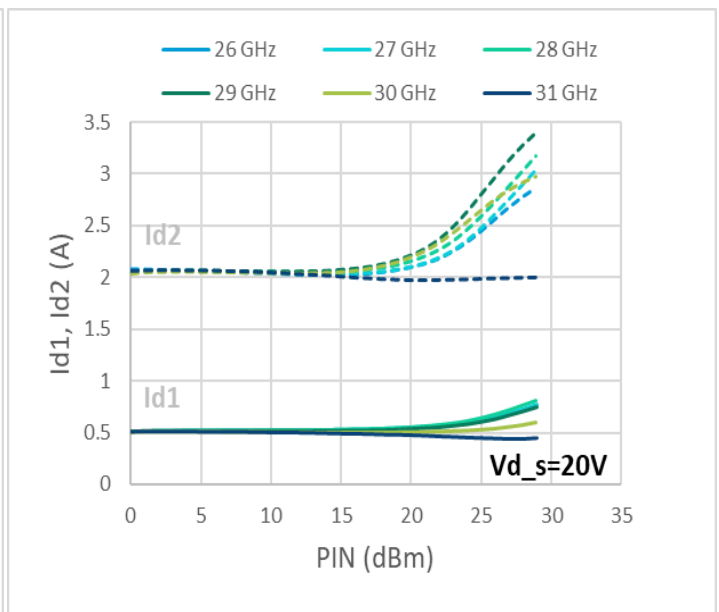
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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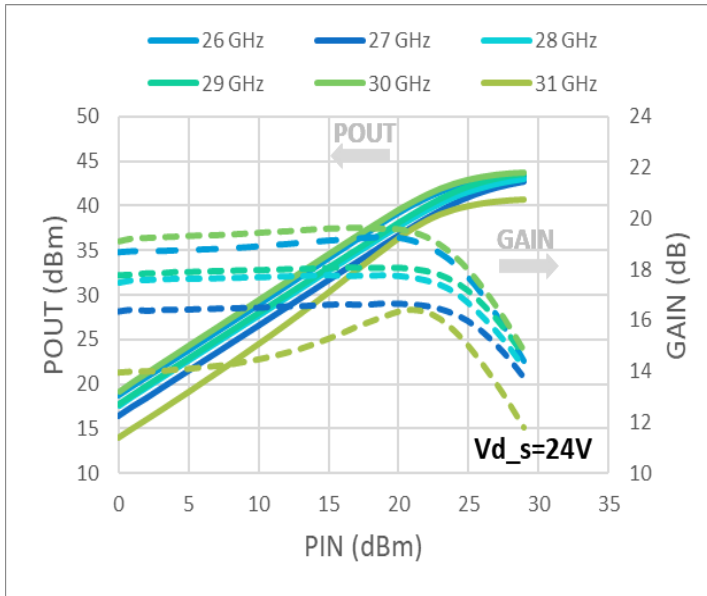
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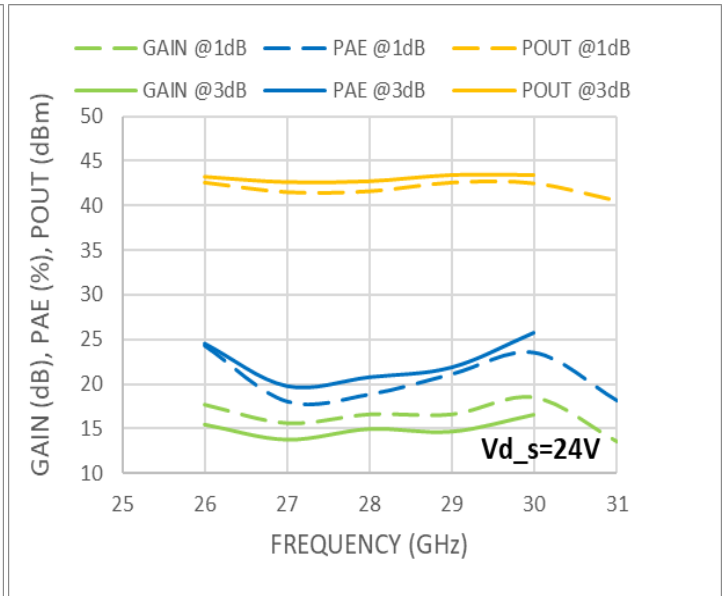
Fixture measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 24.0\text{ V}$, $I_{d1} + I_{d1a} = 520\text{ mA}$, $I_{d2} + I_{d2a} = 2100\text{ mA}$

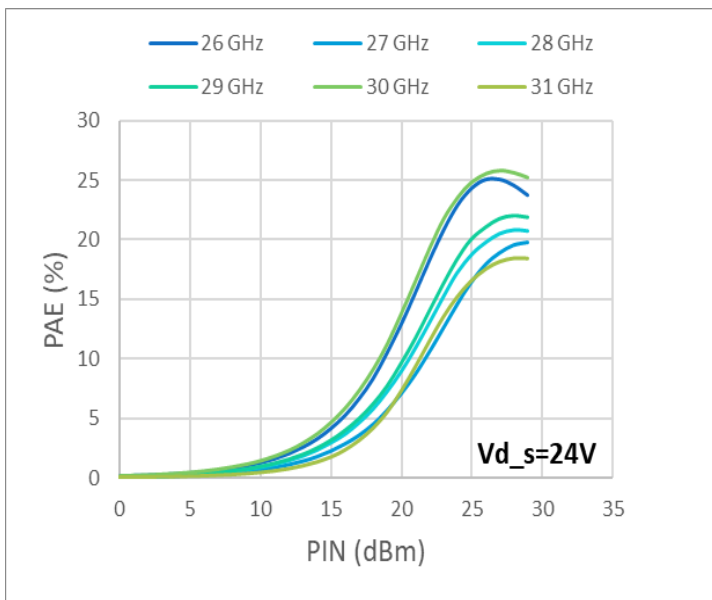
POUT and Gain vs. PIN



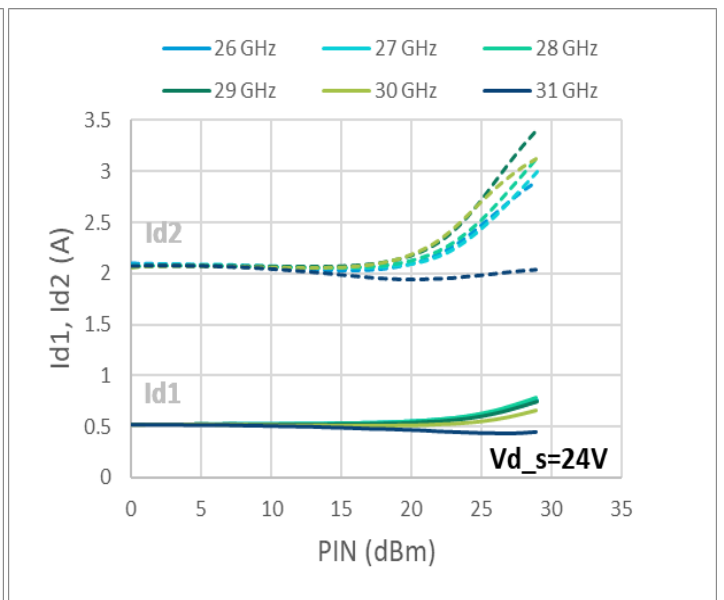
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



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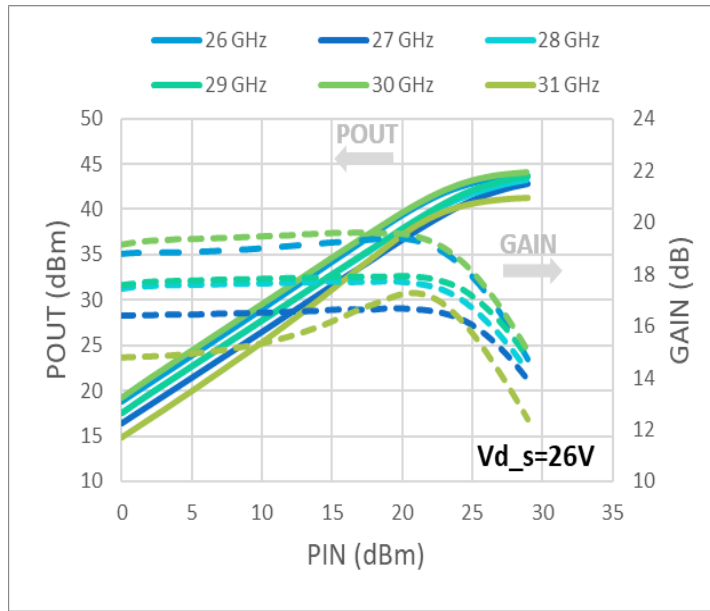
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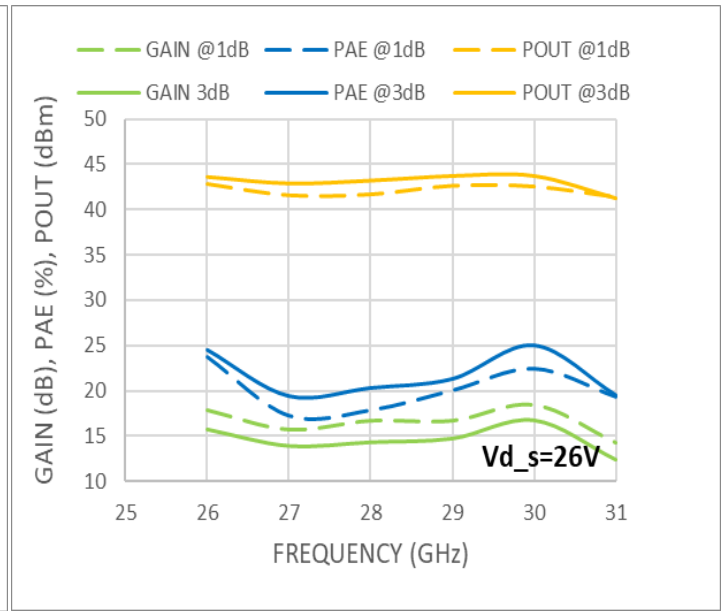
Fixture measured Performance Characteristics (Typical Performance at 25°C)

$V_d = 26.0\text{ V}$, $I_{d1} + I_{d1a} = 520\text{ mA}$, $I_{d2} + I_{d2a} = 2100\text{ mA}$

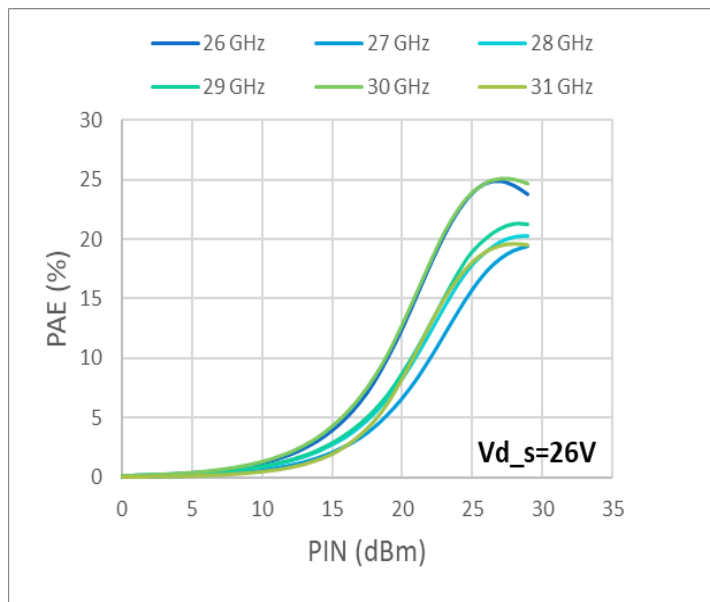
POUT and Gain vs. PIN



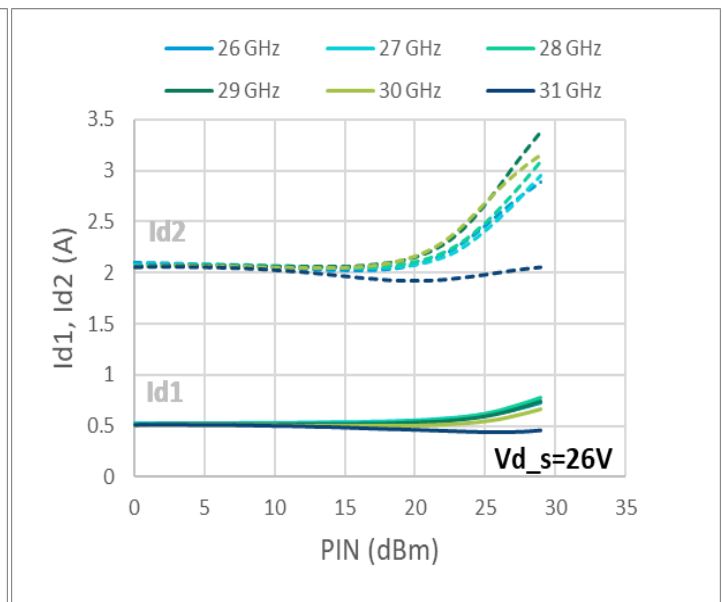
PAE, Gain, POUT vs. Frequency



PAE vs. PIN



ID1, ID2 vs. PIN



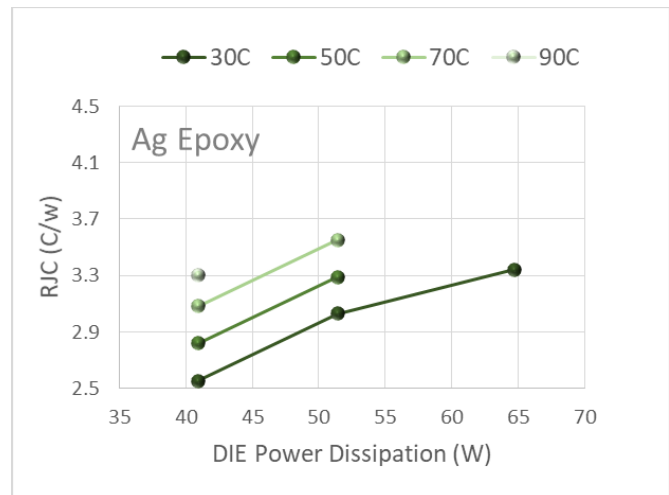
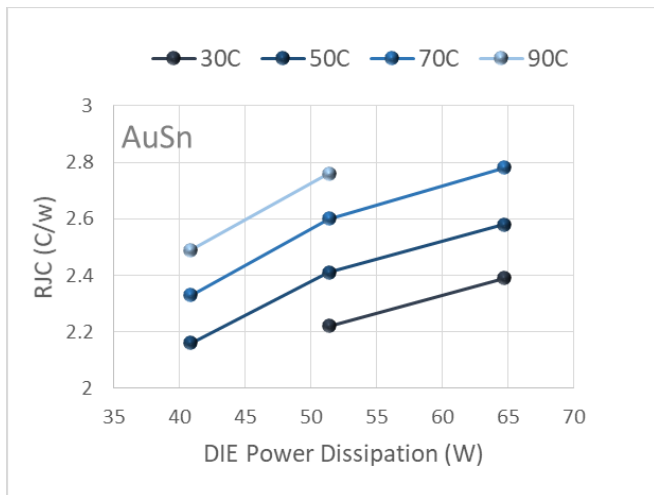
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Preliminary Thermal Properties with die mounted with 25um 80/20 AuSn Eutectic to: 10mil Cu10W Shim

Shim	Mounting Material	Average Backside Die Temperature	Hottest Junction Temperature T _{jc}	RF Output	Power Dissipation (W)	Thermal Resistance R _{jc} (°C/W)		
10 mil CuW	AuSn Eutectic	30 °C	114	40.6	51.4	2.2		
			185	43.0	64.7	2.4		
		50 °C	138	37.1	40.9	2.2		
			174	40.6	51.4	2.4		
			217	43.0	64.7	2.6		
		70 °C	165	37.1	40.9	2.3		
			203	40.6	51.4	2.6		
			250	43.0	64.7	2.8		
		90 °C	192	37.1	40.9	2.5		
			232	40.6	51.4	2.8		
		10 mil CuW	Ag Epoxy	30 °C	134	37.1	40.9	2.6
					186	40.6	51.4	3.0
246	43.0				64.7	3.3		
50 °C	165			37.1	40.9	2.8		
	219			40.6	51.4	3.3		
70 °C	196			37.1	40.9	3.1		
	252			40.6	51.4	3.6		
90 °C	225			37.1	40.9	3.3		



** V_d = 24.0 V, I_{dq1} = 520 mA, I_{d2q} = 2100 mA

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DIE SIZE AND BOND PAD LOCATIONS (NOT TO SCALE)

X = 3300 μm \pm 25 μm

Y = 4100 \pm 25 μm

DC Bond Pad = 100 x 100 \pm 0.5 μm

RF Bond Pad = 134 x 208 \pm 0.5 μm

Chip Thickness = 101 \pm 5 μm

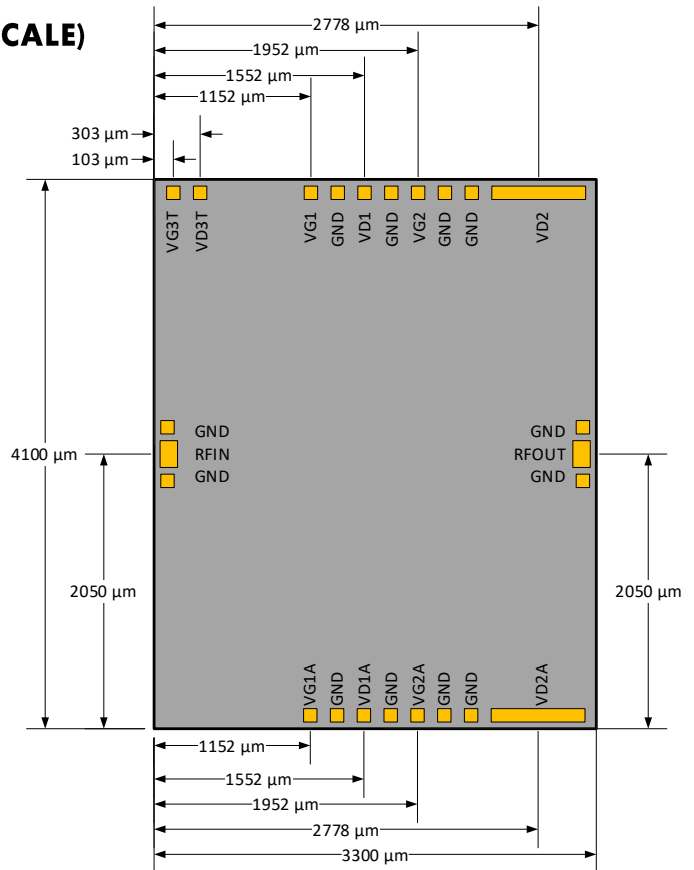
BIASING/DE-BIASING DETAILS:

Bias for 1st stage is from top.

The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

- a. Limited positive gate bias (G-S or G-D) to < 1V
- b. Know your devices' breakdown voltages
- c. Use a power supply with both voltage and current limit
- d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture
 - a. Apply negative gate voltage (-8 V) to ensure that all divides are off
 - b. Ramp up drain bias 10 ~10 V
 - c. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
 - d. Ramp up drain to operating bias
 - e. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
- e. To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
 - a. Set gate voltage back to pinch-off (-8 V)
 - b. Gradually decrease drain bias to 0 V
 - c. Gradually decrease gate bias to 0 V
 - d. Turn off supply voltages
- f. Repeat de-bias procedure for each amplifier stage



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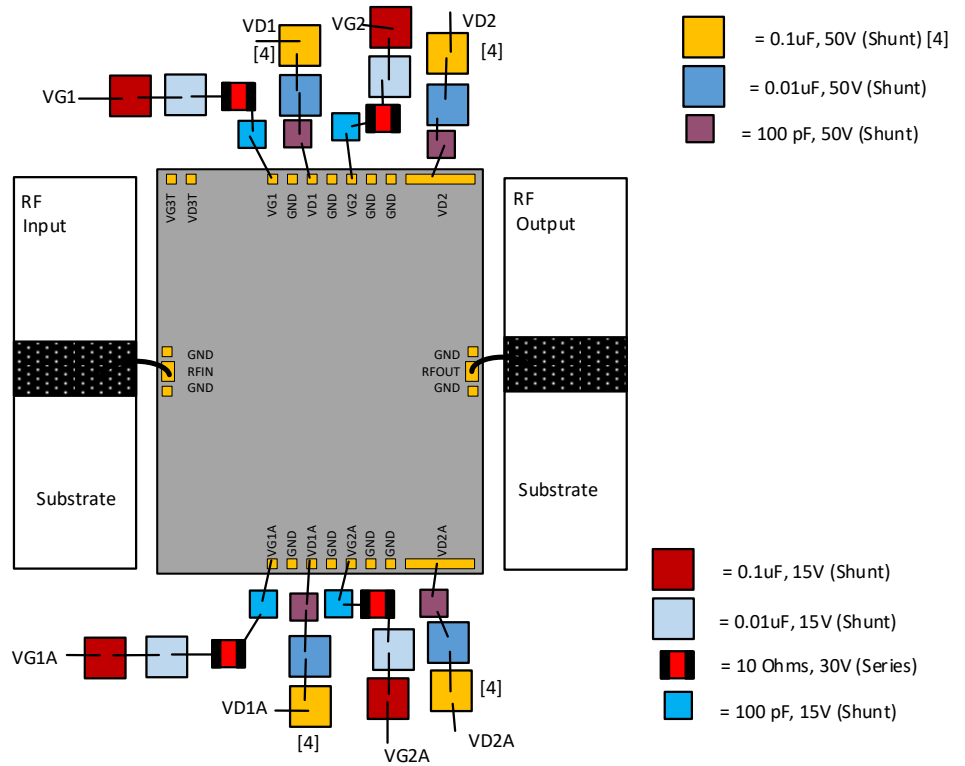
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RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF, 50V Capacitors.

SUGGESTED BONDING ARRANGEMENT



MOUNTING PROCESSES

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320oC for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pickup tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!