

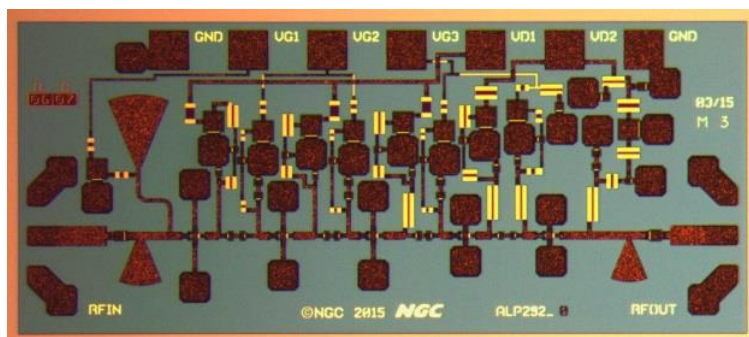
# ALP292

## 90 – 110 GHz

### InP Low Noise Amplifier

## PRODUCT DESCRIPTION

The ALP292 W-band InP HEMT Low Noise Amplifier is a 5-Stage, broadband, ultra low noise amplifier MMIC. It can be used in applications such as W-band commercial digital microwave Links, radios, wireless LANs, Radar, Sensors and Test Equipment. The small die size allows for extremely compact packaging. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression and thermosonic wire bonding assembly techniques.



**X= 1.9 mm; Y= 0.85 mm**

## APPLICATIONS

- W-Band Communication Links
- Short Haul / High Capacity Links
- Radar
- Sensors
- Test & Measurement Systems

## PRODUCT FEATURES

- RF frequency: 90-110 GHz
- Broadband Operation
- Linear gain: 27 dB, typical
- Gain Flatness: 3.5 dB typical
- Noise Figure: 3.1 dB, typical
- P1dB : 3 dBm (Est.)
- Microstrip Topology MMIC, In-line Input & Output
- Die Size 1.62 sq. mm
- 0.1 um InP HEMT Process
- 3 mil substrate
- DC Power: < 35 mW



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#### ABSOLUTE MAXIMUM RATINGS

| Parameter             | Value       | Unit |
|-----------------------|-------------|------|
| Drain Voltage         | 1.3         | V    |
| Gate Voltage Range*   | -0.7 to 0.4 | V    |
| Drain Current         | 30          | mA   |
| Forward Gate Current  | 0.12        | mA   |
| Reverse Gate Current  | -0.3        | mA   |
| Soldering Temperature | 1.3         | V    |

\*Vgd max 2C

#### RECOMMENDED OPERATING CONDITIONS

| Parameter           | Value       | Unit |
|---------------------|-------------|------|
| Drain Voltage Range | 1.3         | V    |
| Gate Voltage Range  | -0.7 to 0.3 | V    |
| Vd1 Drain Current   | 13.5        | mA   |
| Vd2 Drain Current   | 12          | mA   |

#### ELECTRICAL SPECIFICATIONS

| Parameter                        | Min  | Typical | Max  | Unit |
|----------------------------------|------|---------|------|------|
| Operational Frequency            | 90   |         | 110  | GHz  |
| <b>Small Signal S-Parameters</b> |      |         |      |      |
| Small Signal Linear Gain         | 24.5 | 27.0    |      | dB   |
| Gain Flatness                    |      | 3.5     |      | dB   |
| Input Return Loss                |      | -12     | -3.5 | dB   |
| Output Return Loss               |      | -16     | -9   | dB   |
| <b>Noise Figure</b>              |      |         |      |      |
| Operational Frequency*           | 90   |         | 100  | GHz  |
| Noise Figure                     |      | 3.1     | 3.3  | dB   |

\*Noise has been measured only up to 100 GHz

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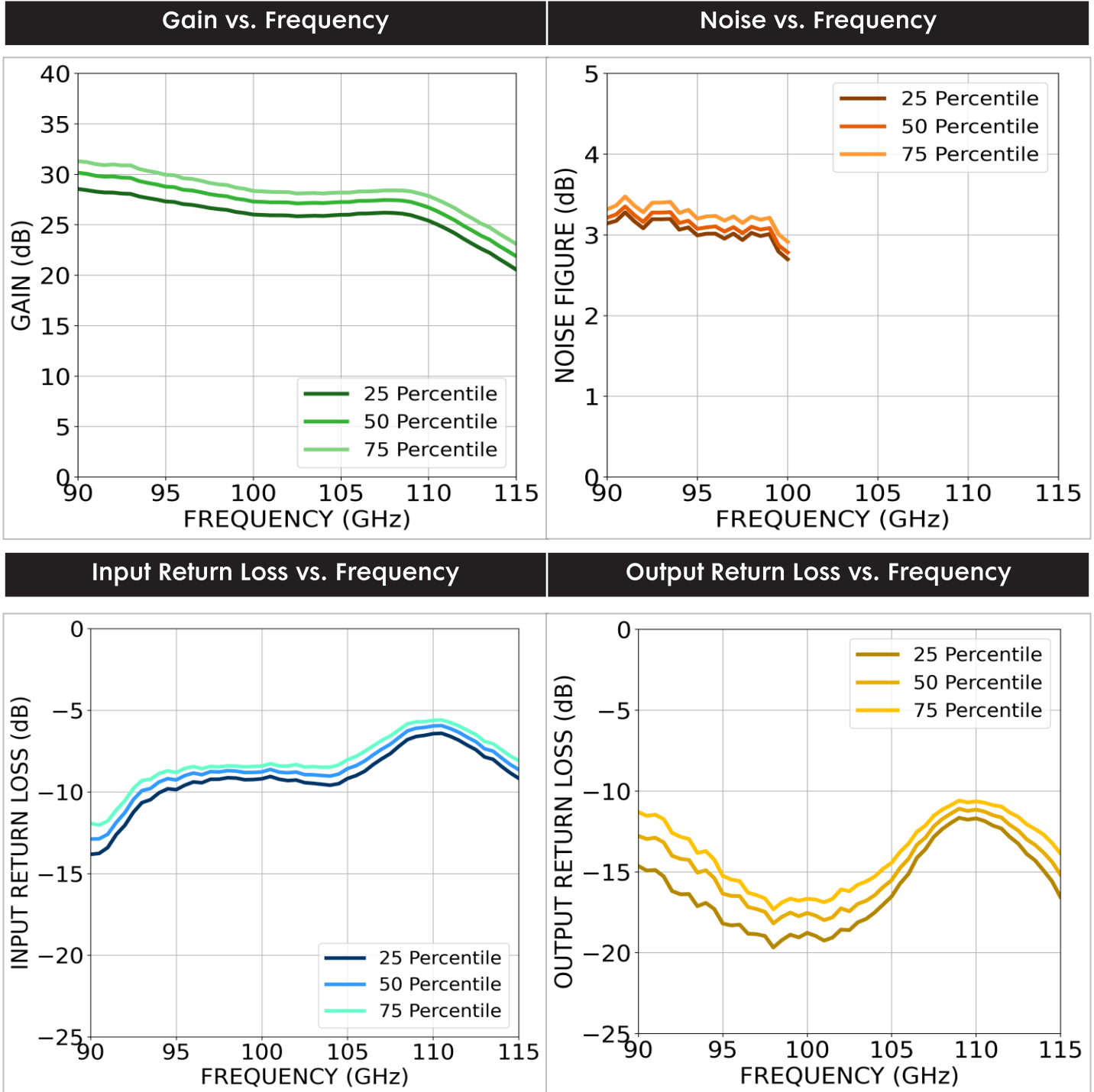
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Pulsed On wafer measured Performance Characteristics (Typical Performance at 25°C)

Vd = 1.3 V, Id1 = 13.5 mA, Id2 = 12 mA. \*



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\* Pulsed-power on-wafer

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## DIE SIZE AND BOND PAD LOCATIONS

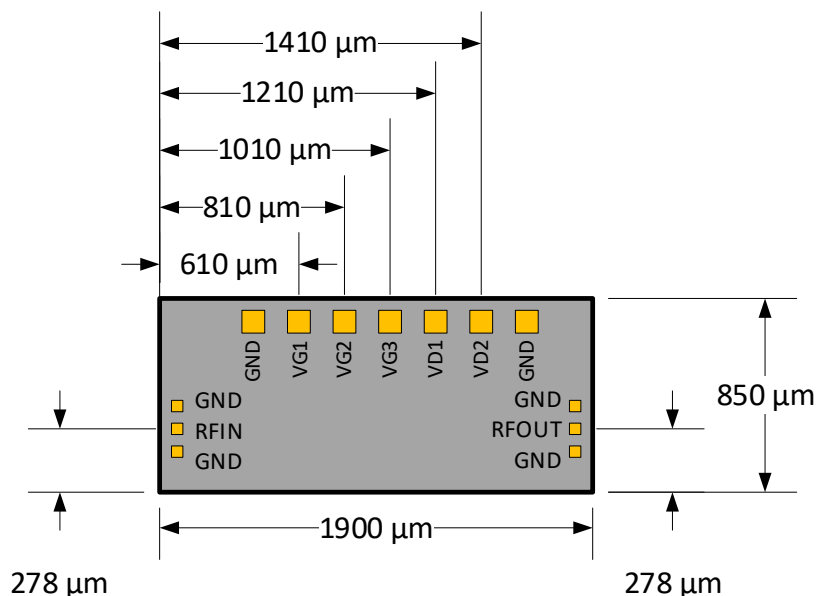
X = 1900  $\mu\text{m}$   $\pm$  25  $\mu\text{m}$

Y = 850  $\pm$  25  $\mu\text{m}$

DC Bond Pad = 100 x 100  $\pm$  0.5  $\mu\text{m}$

RF Bond Pad = 50 x 50  $\pm$  0.5  $\mu\text{m}$

Chip Thickness = 75  $\pm$  5  $\mu\text{m}$



## BIASING/DE-BIASING DETAILS:

Bias up sequence:

- Set all drain and gate voltages to 0V
- Set  $V_{g1} = V_{g2} = V_{g3}$  to -0.7V and check to make sure there is no gate current. High gate current indicates leaky devices.
- Increase  $V_{d1}$  and  $V_{d2}$  to +0.4V and check to make sure there are no oscillations.
- If no oscillations are evident, increase  $V_{d1}$  and  $V_{d2}$  voltage to recommended value (1.3V).
- Adjust  $V_{g1}$  to realize the desired  $I_{d1}$  (4.5mA)
- Adjust  $V_{g2}$  to realize the desired  $I_{d1}$  (13.5mA)
- Adjust  $V_{g3}$  to realize the desired  $I_{d2}$  (12mA)

Bias down sequence:

- Set  $V_{g1} = V_{g2} = V_{g3}$  to -0.7V
- Set  $V_{d1} = V_{d2}$  to 0V
- Set  $V_{g1} = V_{g2} = V_{g3}$  to 0V

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## RECOMMENDED ASSEMBLY NOTES

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <6 mil (long) by 1.5 by 0.5 mil ribbons on input and output.

## SUGGESTED BONDING ARRANGEMENT

### GENERAL DIAGRAM SYMBOLS



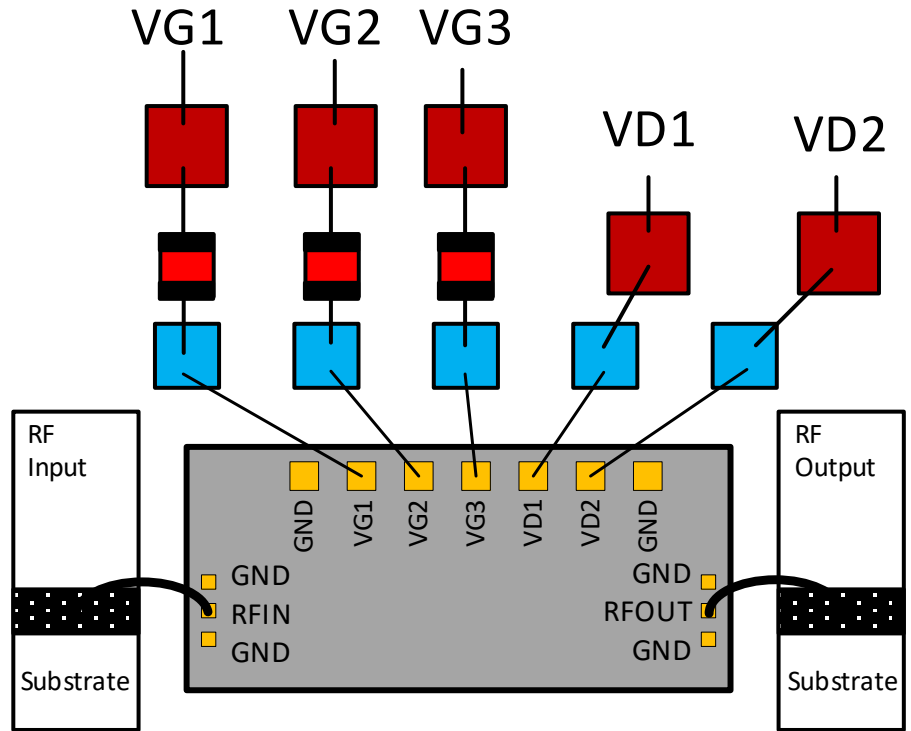
= 100 pF



= 0.1 uF



= 10 Ohms (Series)



## MOUNTING PROCESSES

Most NG InP IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NG recommends the use of conductive epoxy due to the reduced mechanical strain placed on the chip. The two most important factors when mounting these MMICs are to provide a good thermal path and a good RF path to ground. This should be considered when determining the method for attachment.

Note: Many of the NG parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE InP CHIPS.

**PLEASE ALSO REFER TO OUR "GaAs & InP Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICs!**

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