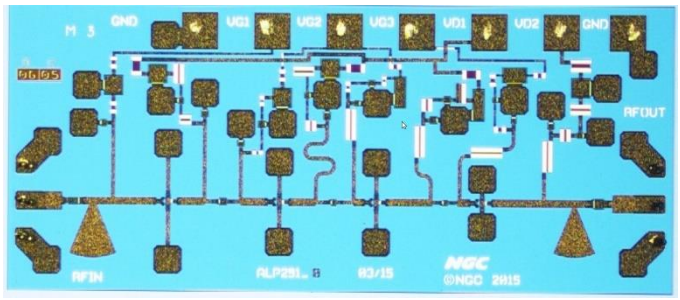
ALP291
71–86 GHz Low Noise Amplifier

Revision 2022-1

NORTHROP GRUMMAN



x=1.9 mm; y=0.85 mm

Product Description

The ALP291 is an E-band low noise amplifier MMIC fabricated in 0.1um InP HEMT. This part is ideally suited for communications. The MMIC operates from 71 to 86 GHz and provides greater than 24 dB of gain with an average noise figure of 2.7 dB. The small die size allows for extremely compact packaging. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Ti/Au, which is compatible with conventional die attach, thermocompression and thermosonic wire bonding assembly techniques

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

Product Features

- Linear gain: 24 - 25 dB, typical
- Noise Figure: 2.5 – 2.9 dB, typical
- Average NF (71-86 GHz): 2.7 dB, typical
- P1dB : 3 dBm (Est.)
- Microstrip Topology MMIC, In-line Input & Output
- 0.1 um InP HEMT Process
- 3 mil substrate
- DC Power: 25 mW
- Die Size 1.6 sq. mm

Export Information
ECCN: **5A991.h**
HTS (Schedule B) code: **8542.33.0000**

Web: http://www.yeswegan.com

Phone: (310) 814-5000 • Fax: (310) 812-7011 • E-mail: as-mps.sales@ngc.com

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Absolute Maximum Ratings

Parameter	Value	Unit
Drain Voltage	1.3	V
Gate Voltage Range*	-0.7 to 0.4	V
Drain Current	18	mA
Forward Gate Current	0.12	mA
Reverse Gate Current	-0.3	mA

*Vgd max is 2V

Recommended Operating Conditions

Parameter	Value	Unit
Drain Voltage Range	1.3	V
Gate Voltage Range	-0.7 to 0.3	V
Vd1 Drain Current	13.5	mA
Vd2 Drain Current	6	mA

Electrical Specifications

Paramter	Min	Typ	Max	Unit
Operational Frequency	71		86	GHz
Small Signal S-parameters				
Small Signal Linear Gain	24.5	28.7		dB
Gain Flatness			4.5	dB
Input Return Loss		-11.3	-5	dB
Output Return Loss		-22.5	-13	dB
Noise Figure				
Operation Frequency	75		86	GHz
Noise Figure		2.7	3.2	dB

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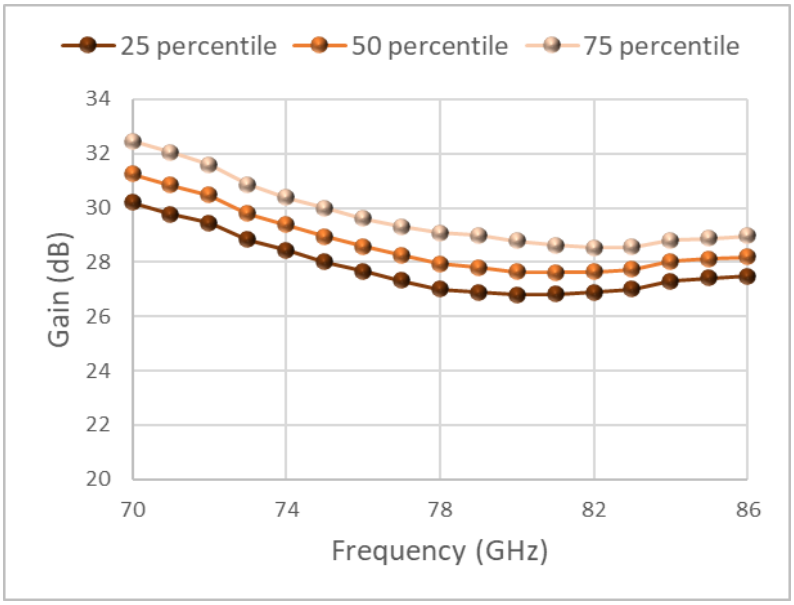
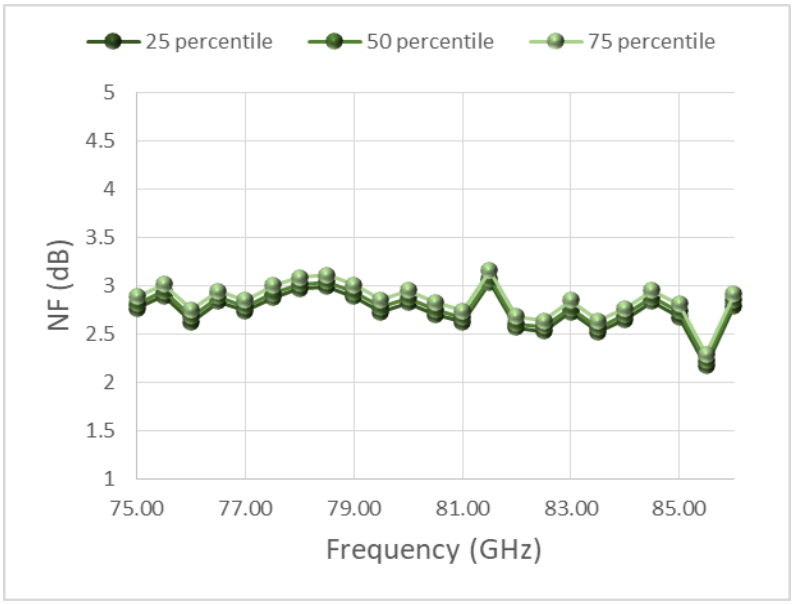
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 1.3V, Id1 = 13.5 mA, Id2 = 6 mA

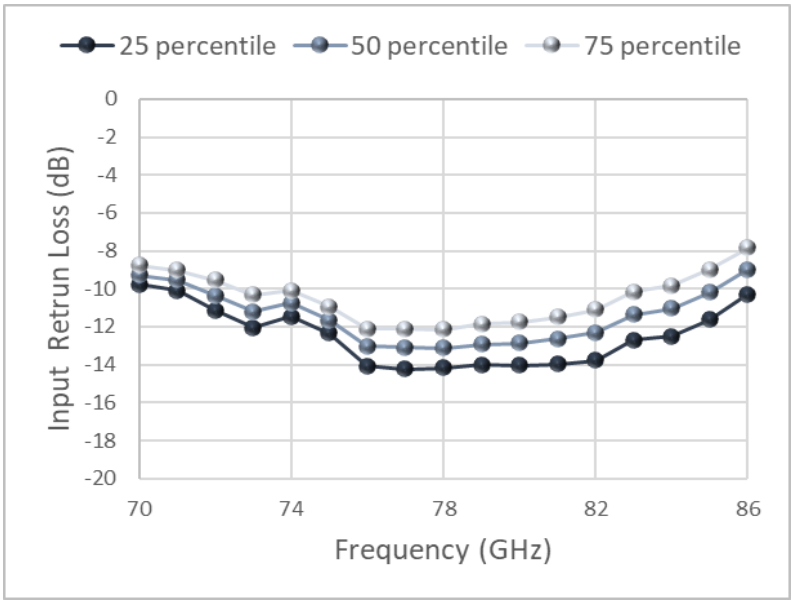
GAIN vs. Frequency



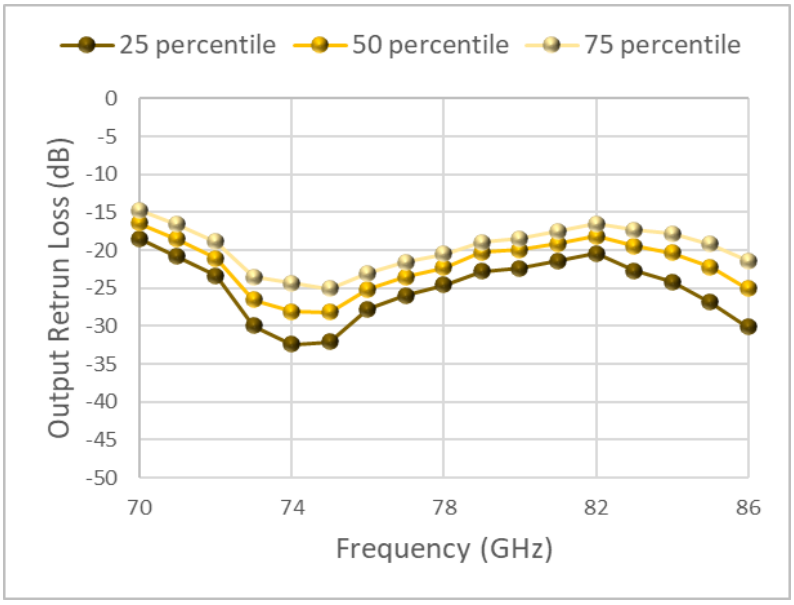
Noise vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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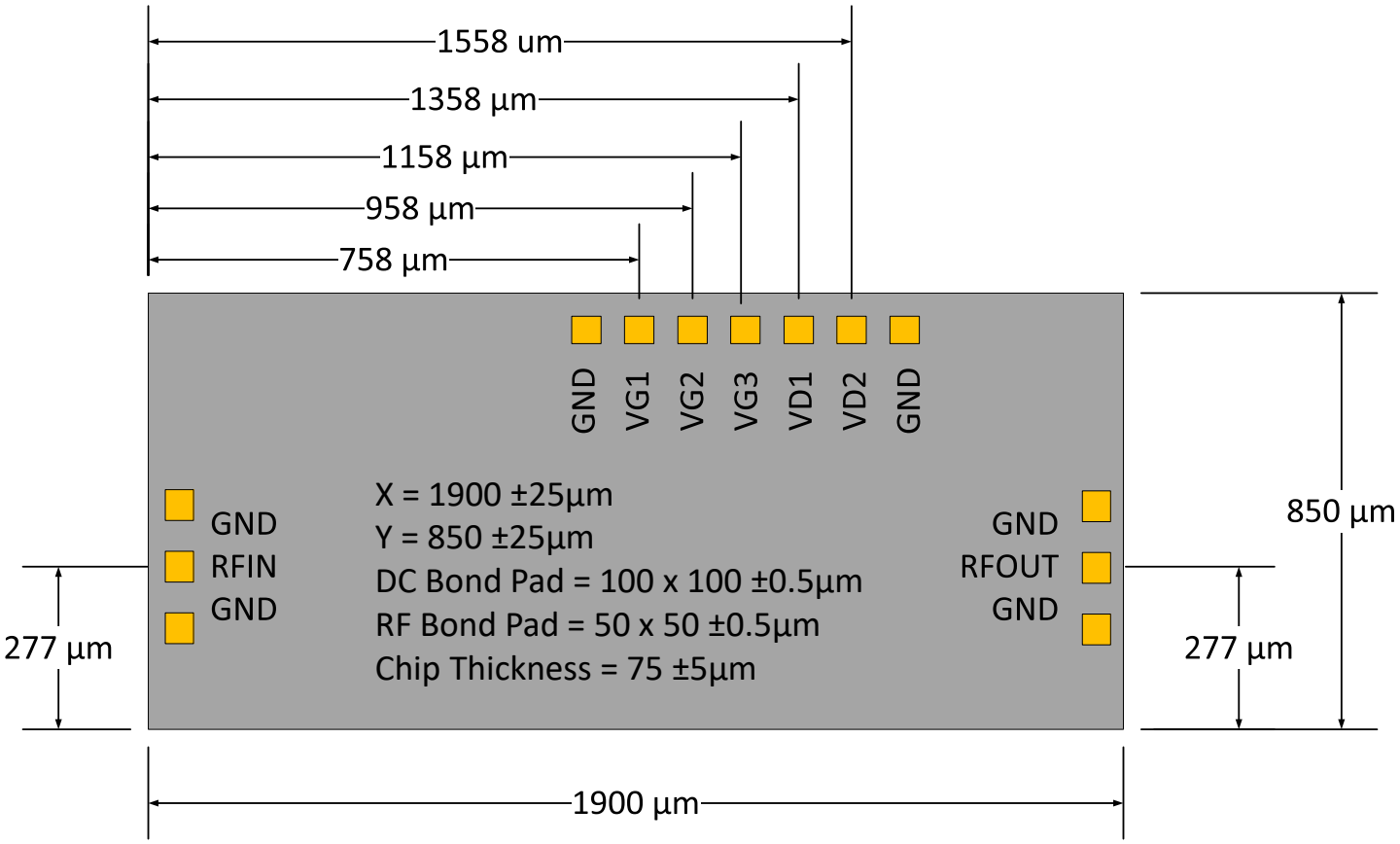
Die Size and Bond Pad Locations (Not to Scale)



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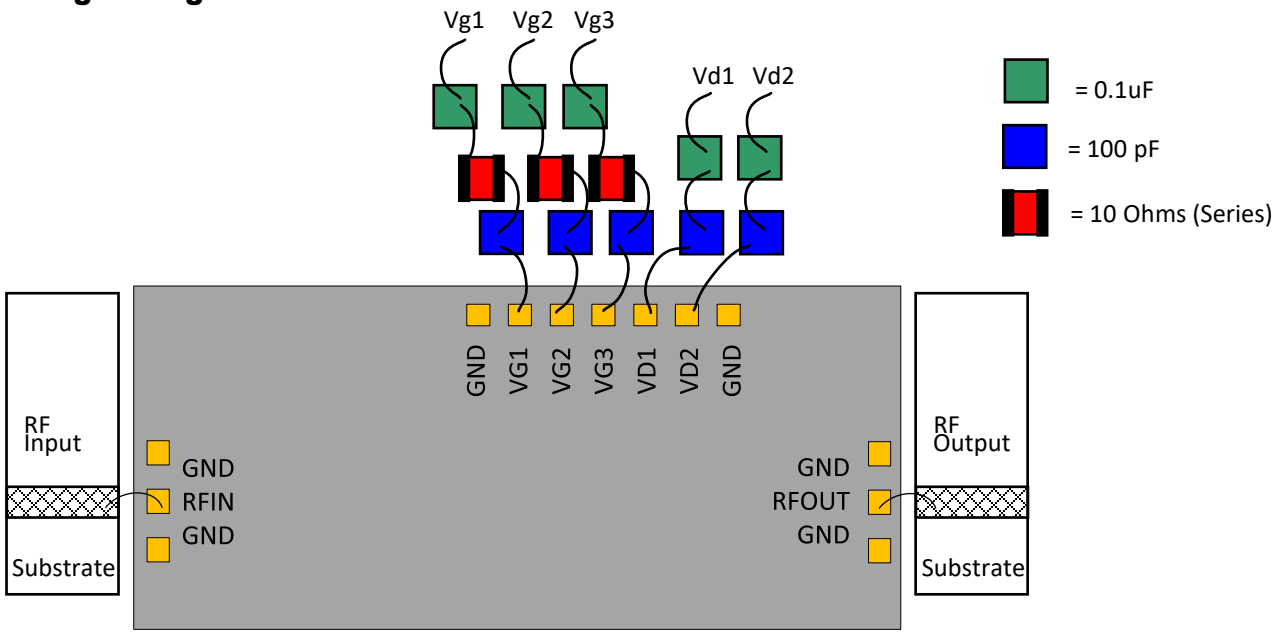
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100pF (approximately) ceramic (single-layer) placed no further than 30 mils from the amplifier.
2. Best performance obtained from use of <6 mil (long) by 1.5 by 0.5 mil ribbons on input and output

Biasing/De-Biasing Details:

Bias up sequence:

- Set all drain and gate voltages to 0V
- Set Vg1 = Vg2 = Vg3 to -0.7V and check to make sure there is no gate current. High gate current indicates leaky devices.
- Increase Vd1 and Vd2 to +0.4V and check to make sure there are no oscillations.
- If no oscillations are evident, increase Vd1 and Vd2 voltage to recommended value (1.3V).
- Adjust Vg1 to realize the desired Id1 (4.5mA)
- Adjust Vg2 to realize the desired Id1 (13.5mA)
- Adjust Vg3 to realize the desired Id2 (6mA)

Bias down sequence:

- Set Vg1 = Vg2 = Vg3 to -0.7V
- Set Vd1 = Vd2 to 0V
- Set Vg1 = Vg2 = Vg3 to 0V

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