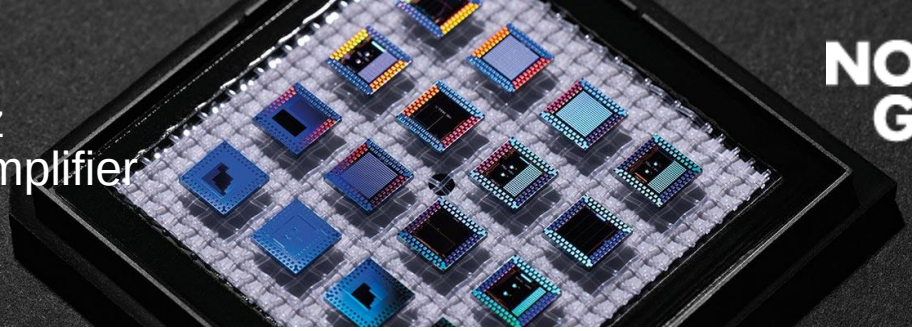
APN236
34.5-35.5 GHz
GaN Power Amplifier



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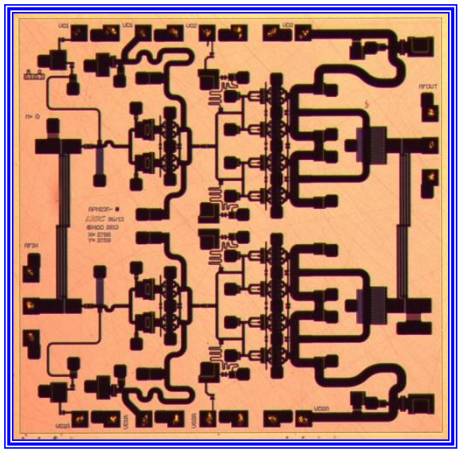

X = 2.7 mm Y = 2.65 mm

Applications

- Military Radar Systems

Product Features

- RF frequency: 34.5 to 36.5 GHz
- Linear Gain: 16 dB typ.
- Psat (est): 40 dBm typ.
- PAE @ Psat typ.: 24%
- Die Size: 7.155 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 996 mA

Product Description

The APN236 monolithic GaN HEMT amplifier is a broadband, balanced two-stage power device, designed for use Military Radar Systems. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	34.5		35.5	GHz
Linear Gain	15	16		dB
Input Return Loss	14	16		dB
Output Return Loss	9	11		dB
P1dB (Pulsed)*		38		dBm
P1dB (CW)**		37.5		dBm
Psat (Pulsed)*		40		dBm
Psat (CW)**		39.5		dBm
PAE @ Psat		24		%
Vd1, Vd1a, Vd2, Vd2a		28		V
Vg1, Vg1a, Vg2, Vg2a		-3.5		V
Id1+ Id1a		256		mA
Id2,+Id2a		740		mA

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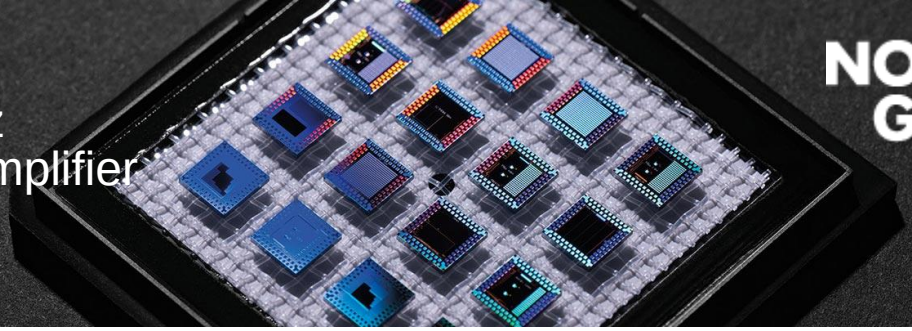

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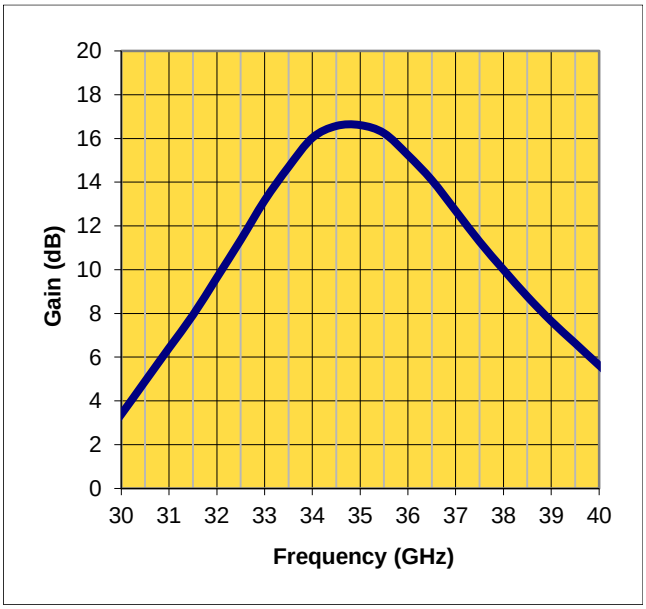
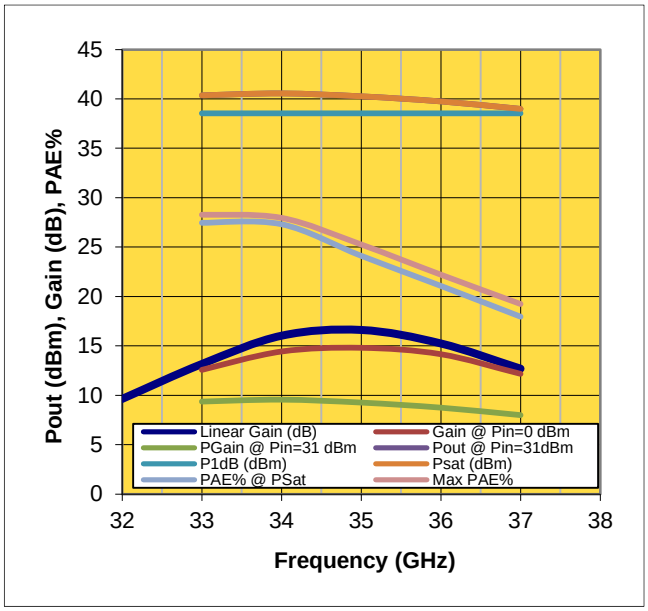
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd1a, Vd2, Vd2a = 28 V, Id1+ Id1a = 256 mA, Id2+Id2a = 740 mA. *

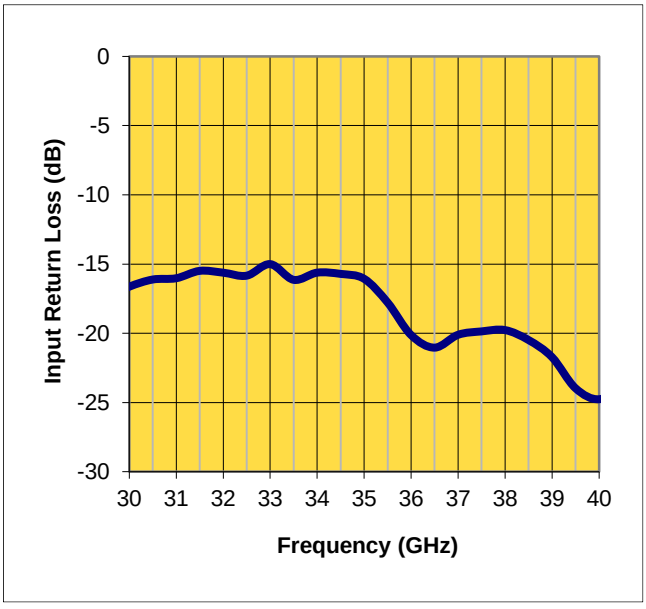
GAIN vs. Frequency



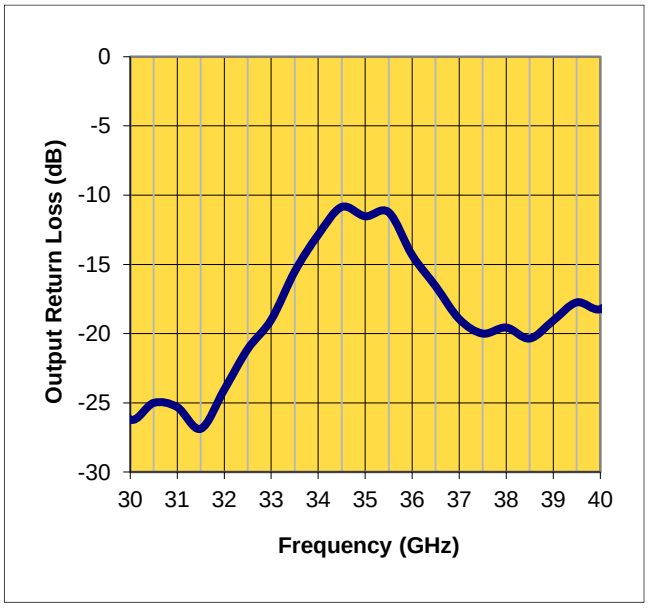
PAE, GAIN, Pout vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



*Pulsed-power on-wafer

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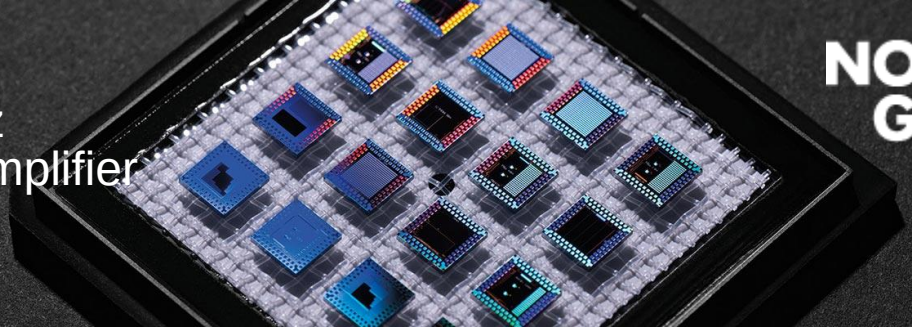

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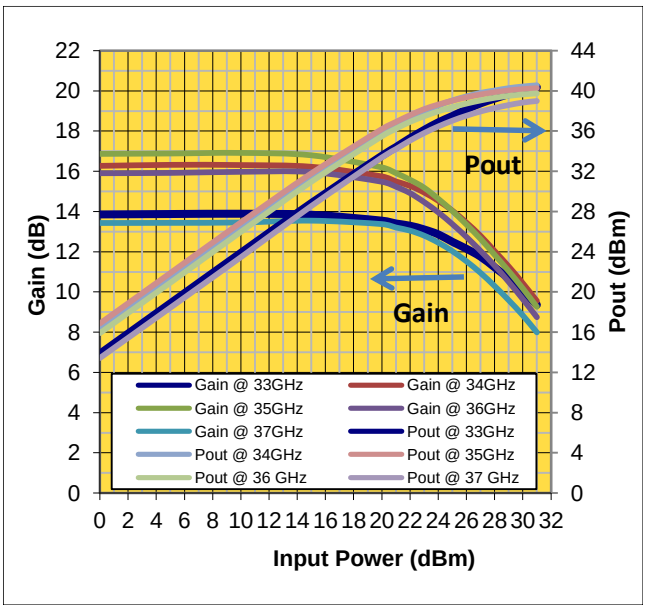
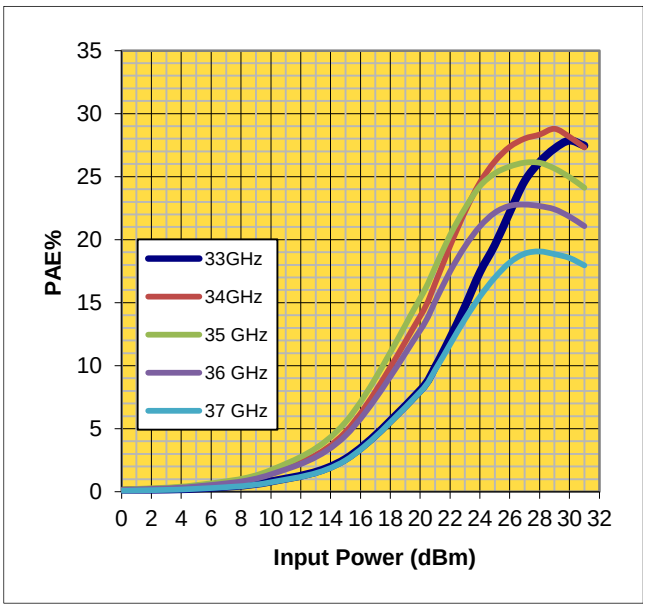
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd1a, Vd2, Vd2a = 28 V, Id1+ Id1a = 256 mA, Id2+Id2a = 740 mA. *

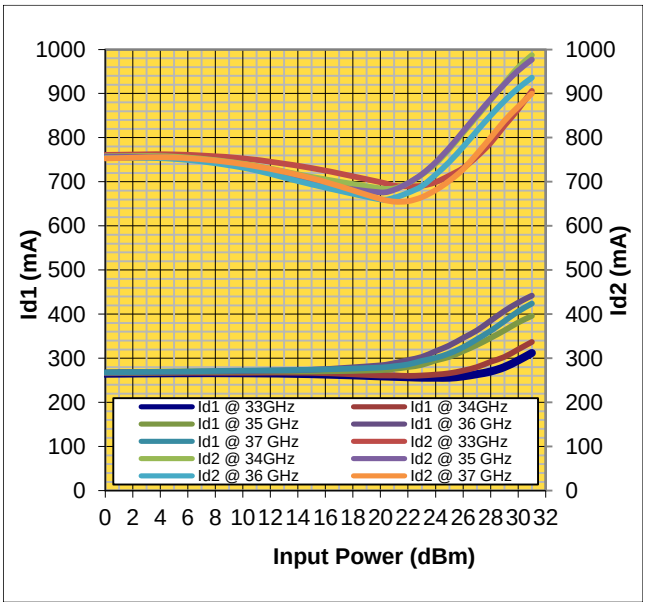
GAIN, Pout vs. Pin



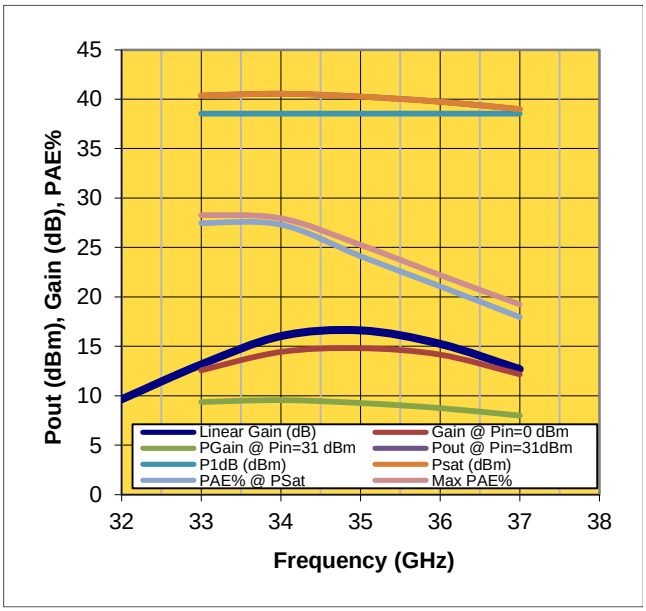
PAE vs. Pin



Id1 vs Pin



Pout, Gain, PAE vs Frequency



*On-wafer Pulsed Power

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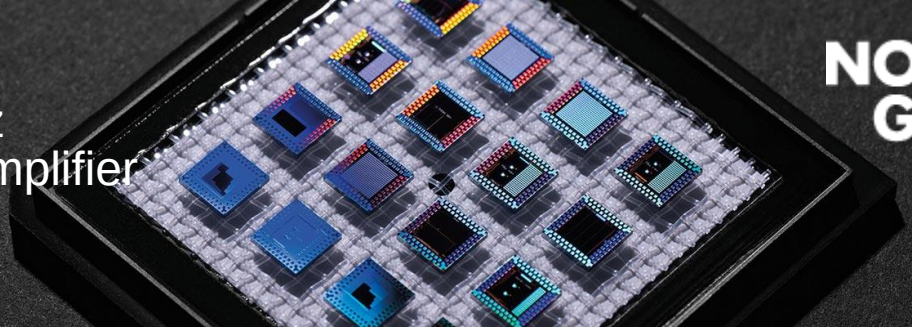

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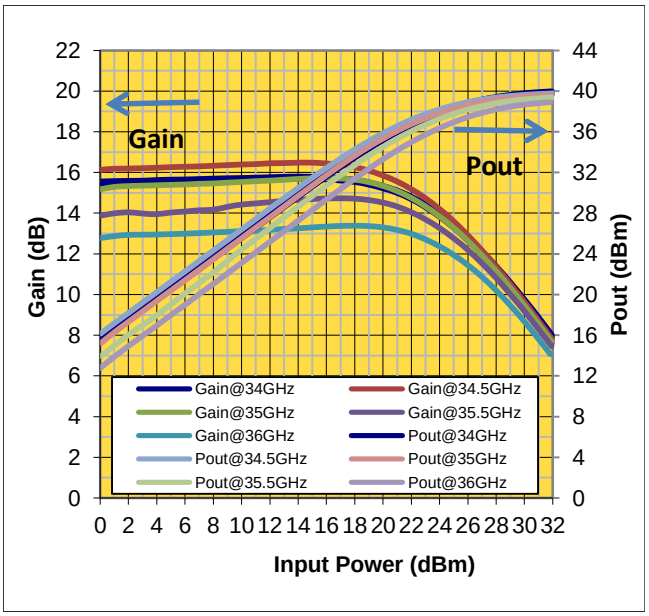
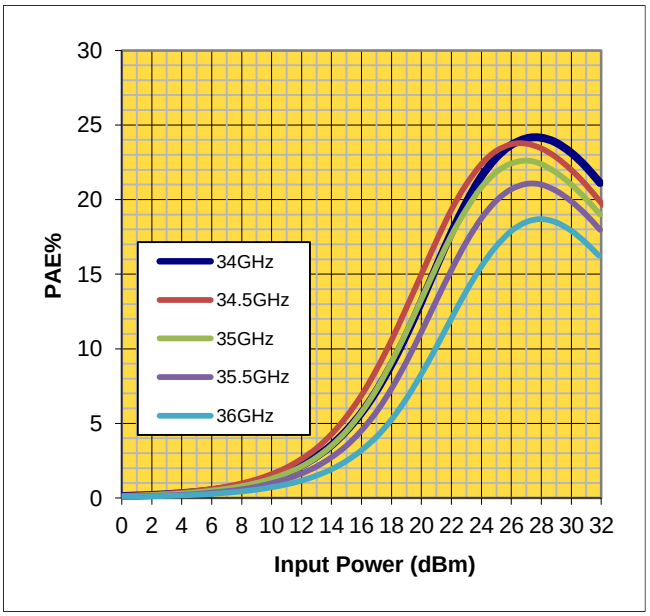
Measured Fixture Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd1a, Vd2, Vd2a = 28 V, Id1+ Id1a = 256 mA, Id2+Id2a = 740 mA. *

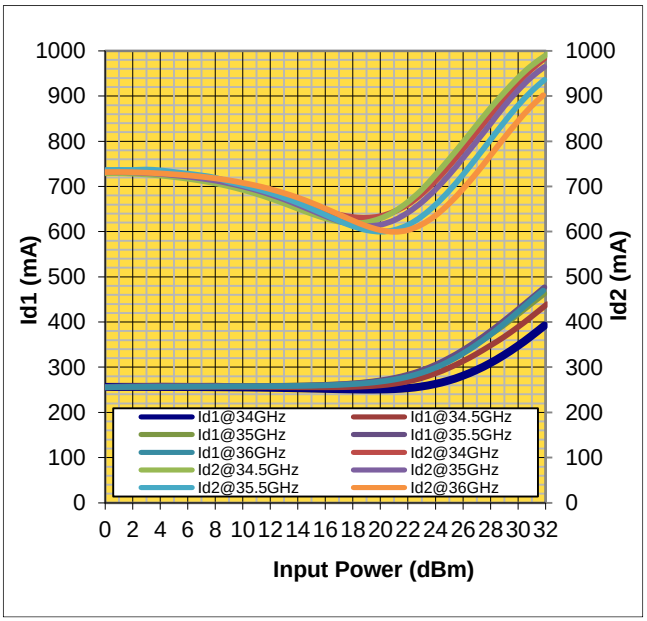
GAIN, Pout vs. Pin



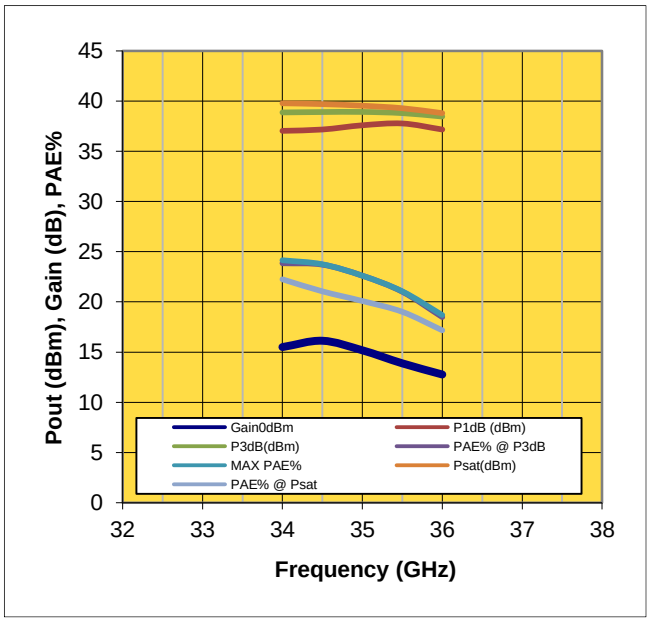
PAE vs. Pin



Id1 vs Pin



Pout, Gain, PAE vs Frequency



*CW Fixture

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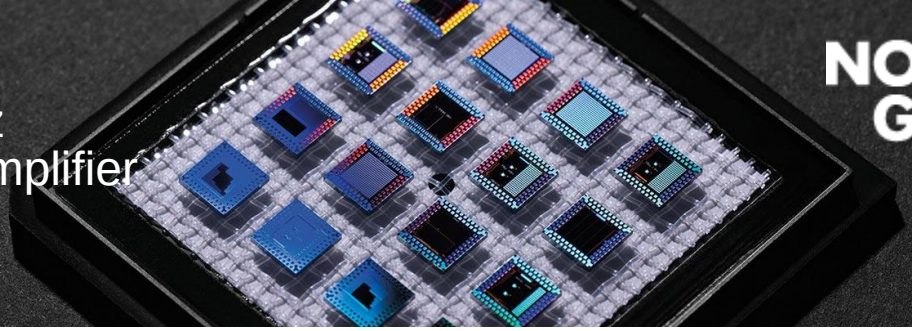

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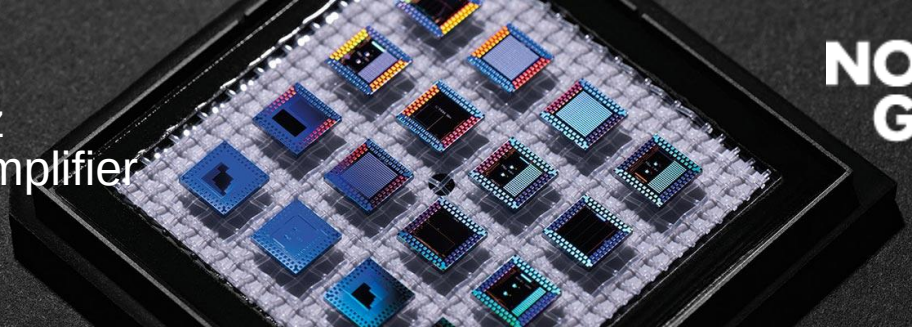
On wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd1, Vd1a, Vd2, Vd2a = 28 V, Id1+ Id1a = 256 mA, Id2+Id2a = 740 mA. *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
27.0	0.062	-129.237	0.551	90.459	0.010	177.923	0.116	160.920
27.5	0.077	-125.081	0.649	76.292	0.005	-126.794	0.113	141.866
28.0	0.089	-124.663	0.761	61.180	0.007	171.615	0.114	139.036
28.5	0.106	-125.311	0.902	45.683	0.007	-17.647	0.107	126.936
29.0	0.117	-130.964	1.065	29.516	0.017	67.959	0.070	111.208
29.5	0.128	-130.821	1.249	12.396	0.006	-1.088	0.062	103.935
30.0	0.143	-136.975	1.476	-4.753	0.009	-8.184	0.049	96.472
30.5	0.149	-142.520	1.751	-22.671	0.009	-29.238	0.039	86.803
31.0	0.154	-145.023	2.077	-41.829	0.012	61.068	0.036	90.848
31.5	0.163	-149.449	2.479	-61.162	0.022	-38.946	0.022	90.737
32.0	0.157	-158.027	3.009	-81.541	0.009	-39.383	0.042	68.986
32.5	0.156	-156.492	3.673	-104.231	0.010	-36.304	0.076	44.451
33.0	0.175	-166.626	4.510	-129.040	0.008	-38.664	0.097	24.045
33.5	0.158	-169.736	5.423	-157.652	0.005	-73.290	0.166	-7.068
34.0	0.171	-172.923	6.199	171.300	0.009	170.415	0.206	-33.959
34.5	0.170	-179.975	6.789	138.762	0.007	162.191	0.287	-57.177
35.0	0.163	170.699	6.843	104.802	0.005	-44.847	0.285	-88.319
35.5	0.133	159.436	6.597	72.388	0.002	-169.966	0.288	-114.610
36.0	0.099	160.157	5.923	41.110	0.002	-152.664	0.200	-131.942
36.5	0.096	176.977	5.214	11.642	0.019	97.367	0.148	-151.591
37.0	0.097	174.694	4.457	-14.876	0.007	-64.029	0.135	-143.436
37.5	0.098	173.890	3.794	-39.019	0.013	90.975	0.101	-140.993
38.0	0.103	170.171	3.254	-62.351	0.001	-124.170	0.109	-124.125
38.5	0.091	163.837	2.792	-84.302	0.005	53.455	0.104	-119.409
39.0	0.080	159.494	2.428	-105.377	0.016	25.244	0.108	-120.721
39.5	0.053	165.906	2.147	-125.734	0.013	15.571	0.127	-126.500
40.0	0.050	-166.535	1.912	-146.866	0.015	-40.561	0.116	-140.360
40.5	0.056	-156.522	1.704	-167.600	0.017	117.350	0.145	-129.641
41.0	0.084	-150.528	1.553	171.997	0.019	73.426	0.146	-138.203
41.5	0.106	-158.190	1.443	150.600	0.005	-23.626	0.184	-133.685
42.0	0.121	-168.906	1.381	127.874	0.008	72.289	0.201	-139.224
42.5	0.133	169.169	1.348	100.131	0.006	126.788	0.188	-141.730
43.0	0.105	162.178	1.254	66.104	0.023	165.530	0.197	-136.312

*Pulsed-power on-wafer



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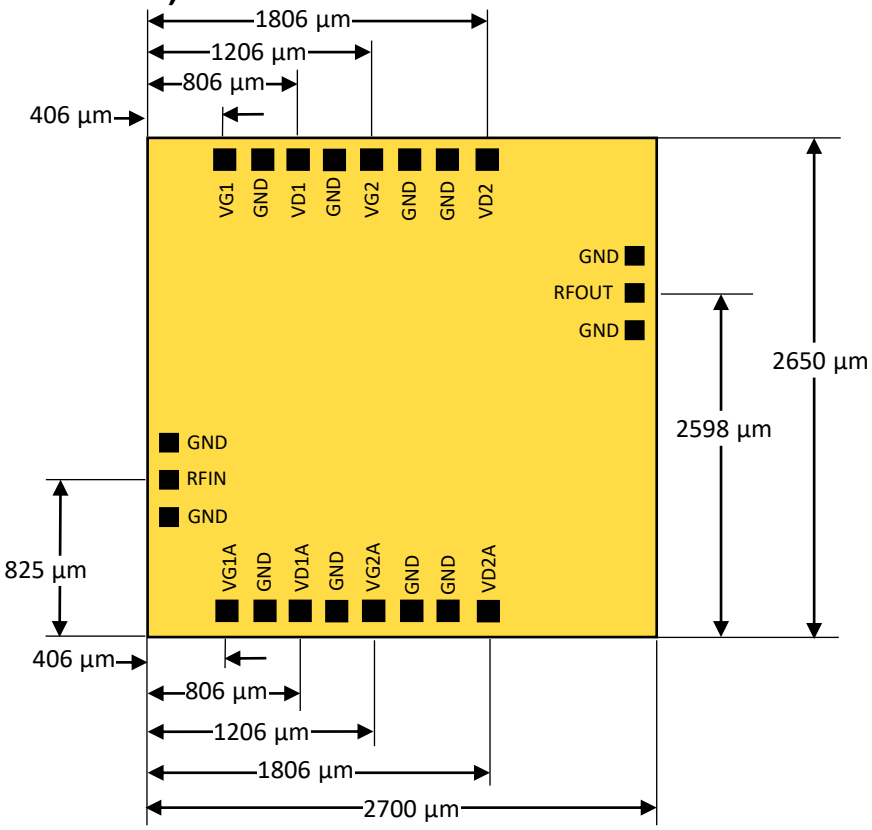
Die Size and Bond Pad Locations (Not to Scale)

X = 2700 ± 25 µm
Y =2650 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

APN236 must be biased the top and bottom of the die.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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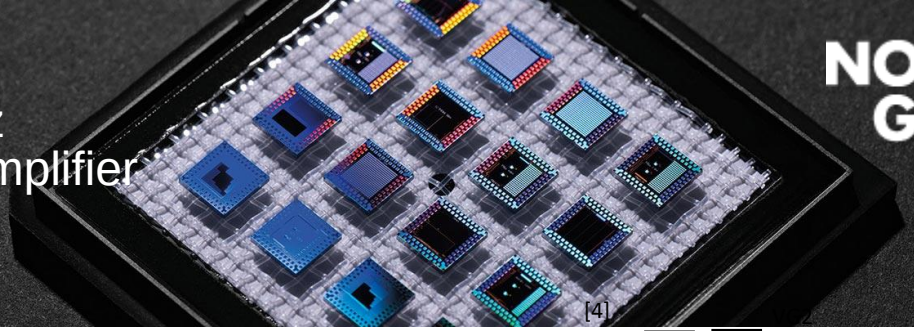

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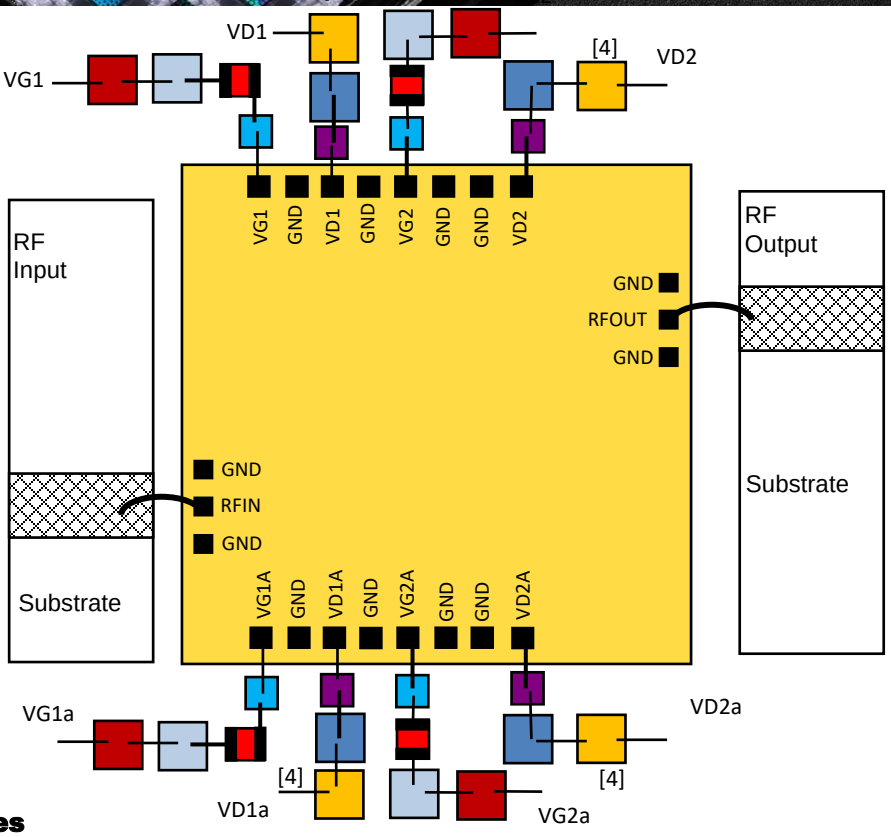
Suggested Bonding Arrangement

= 0.1uF, 50V (Shunt) [4]
= 0.01uF, 50V (Shunt)
= 100 pF, 50V (Shunt)
= 0.1uF, 15V (Shunt)
= 0.01uF, 15V (Shunt)
= 10 Ohms, 30V (Series)
= 100 pF, 15V (Shunt)



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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