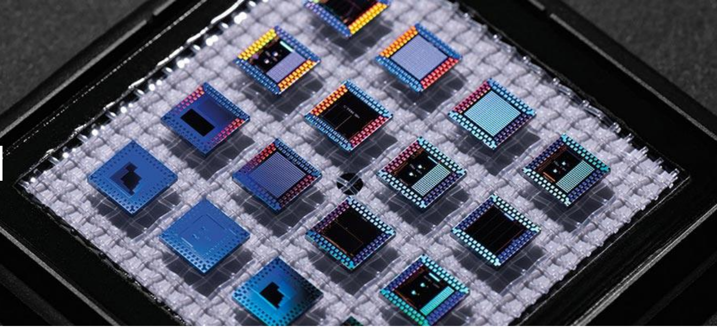
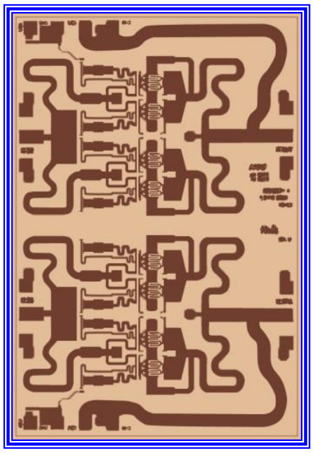
APN237
13.5-15.5 GHz GaN Dual Channel Power Amplifier

NORTHROP GRUMMAN





X = 2.1 mm Y = 3.1 mm

Product Features

- RF frequency: 13.5 to 15.5 GHz
- Dual Channel amplifier allows for easy off-chip power combining
- Single Channel Linear Gain*: 13 dB typ.
- Psat:
  - Combined (est)**: 44.5 dBm PP / 44 dBm CW typ. ***
  - Single Channel: 42 dBm PP / 41.5 dBm CW Typ. ***
- PAE% @ Psat*: 43% PP / 30% CW typ. ***
- Die Size: 6.51 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1280 mA

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SATCOM Terminals

Product Description

The APN237 monolithic GaN HEMT amplifier is a dual channel broadband, two-stage power device, designed for use in SATCOM Terminals and point-to-point digital radios. It is intended for use with external combiners, could used as two independent PAs. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	13.5		14	GHz
Linear Gain**	12	13		dB
Input Return Loss**	7	10		dB
Output Return Loss**	5	9		dB
P1dB (PP**)		40.5		dBm
P1dB (CW**)		38.8		dBm
Psat (PP**)		44.5		dBm
Psat (CW**)		44		dBm
PAE @ Psat (PP**)		43		%
PAE @Psat (CW**)		30		%
Vd1, Vd1a		28		V
Vg1, Vg1a		-3.5		V
Id1+Id1a		1280		mA

* Single Channel   ** Assuming Optimal combining *** @ Vd=28V

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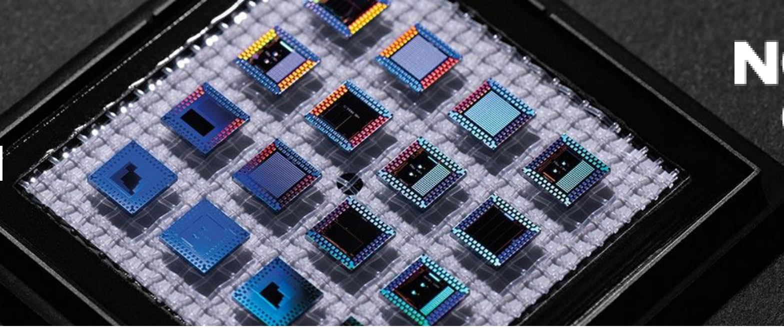
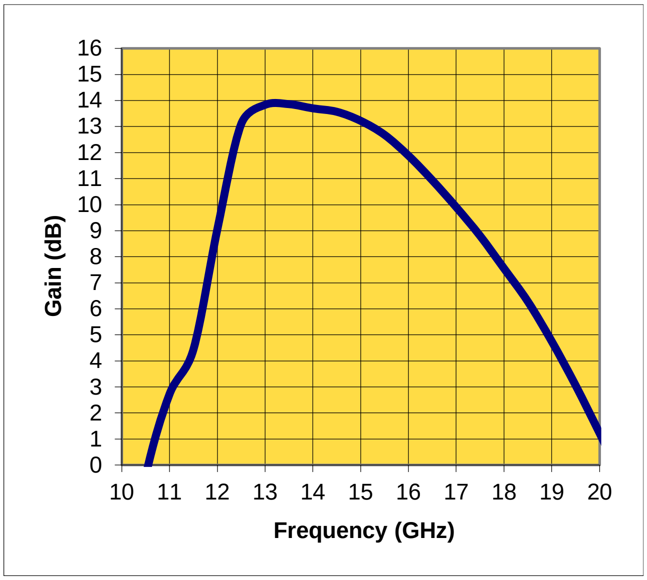
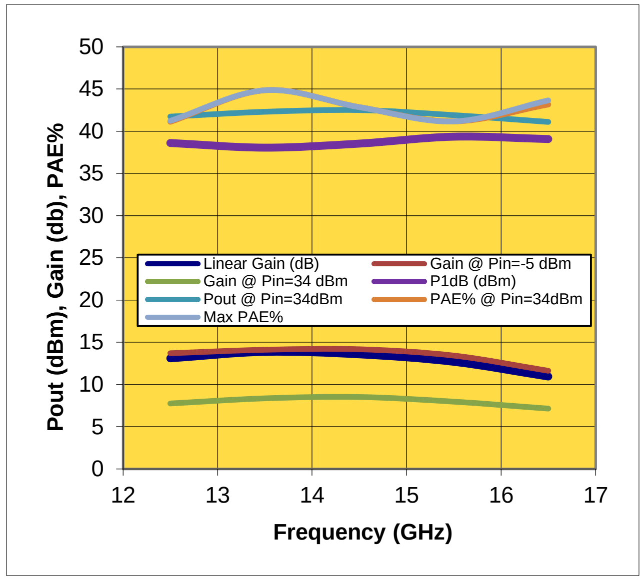


On-wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. (single channel) *

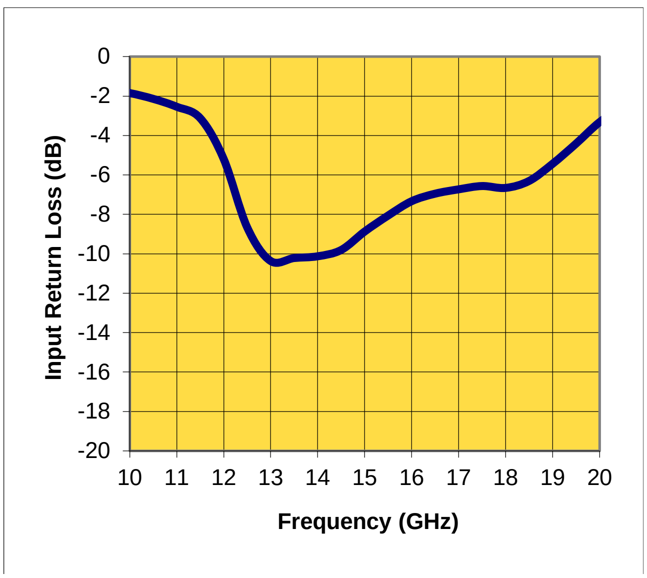
GAIN vs. Frequency



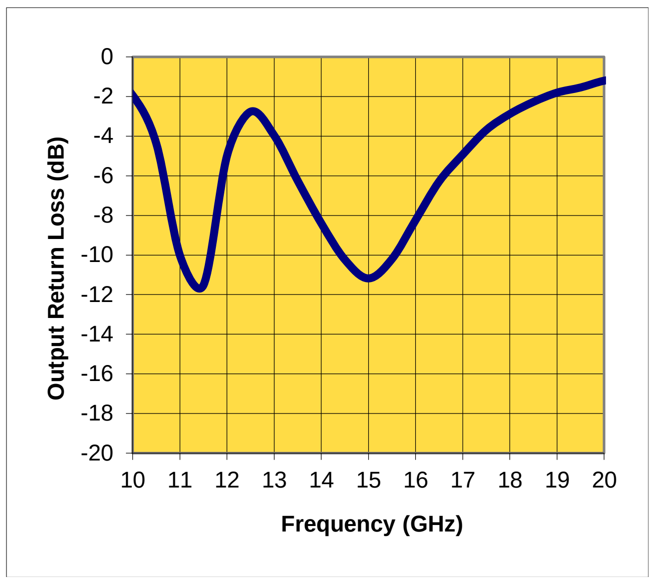
PAE, GAIN, Pout vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



*Pulsed-power on-wafer

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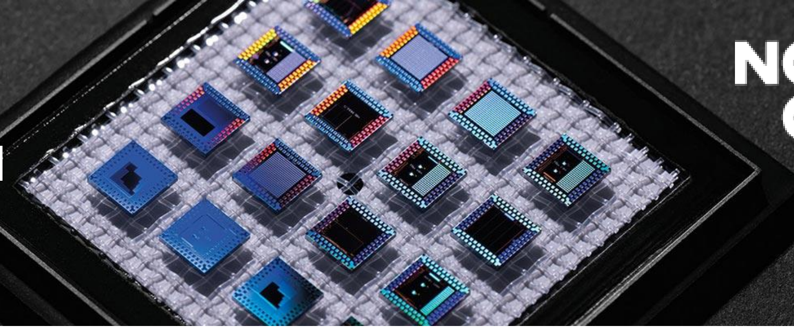

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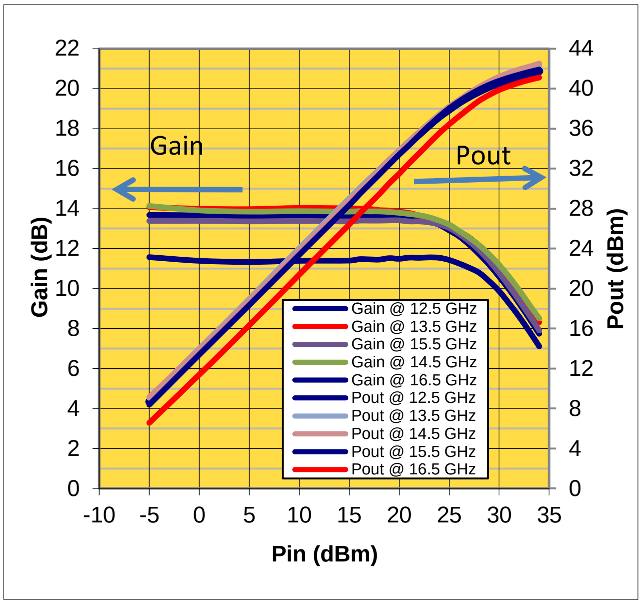
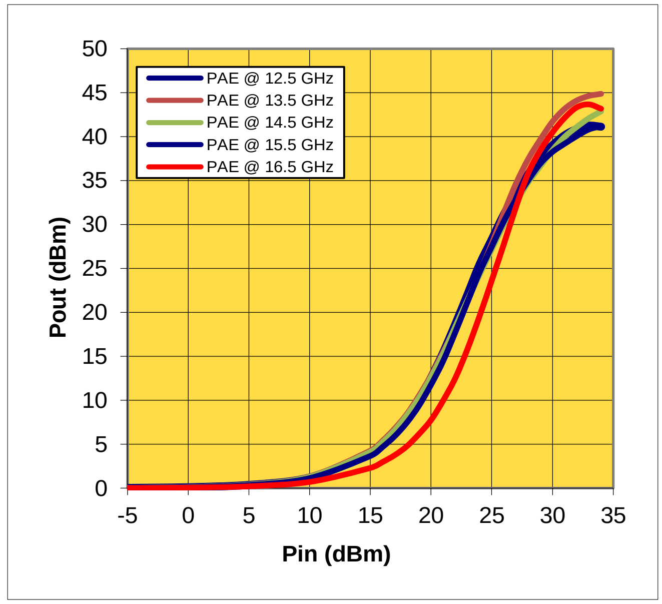
On-wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. *

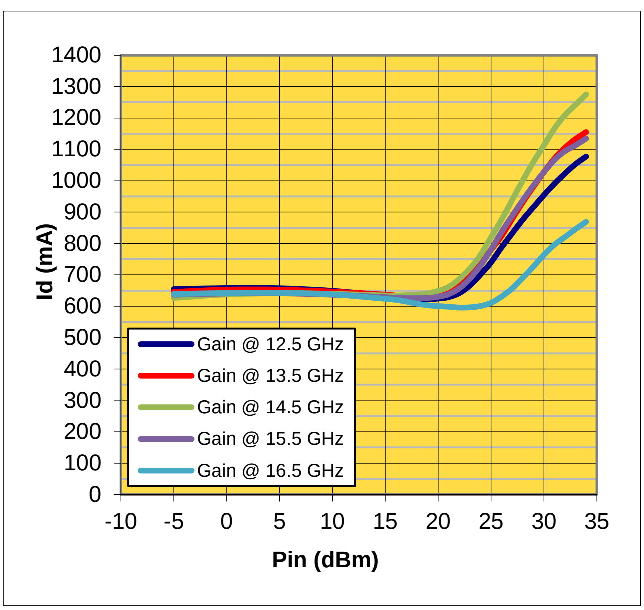
GAIN, Pout vs. Pin



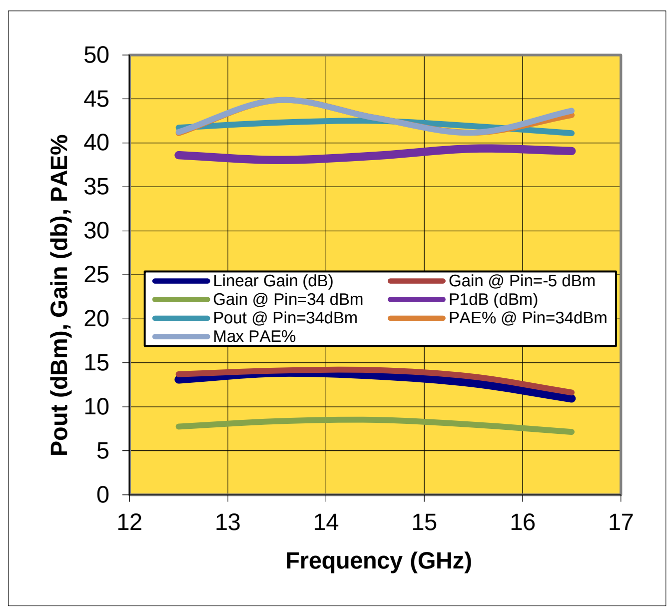
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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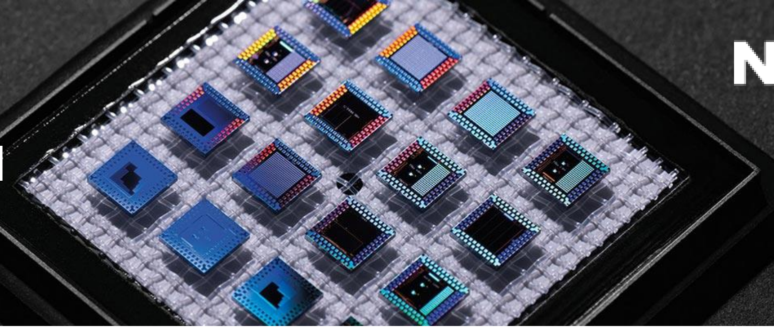
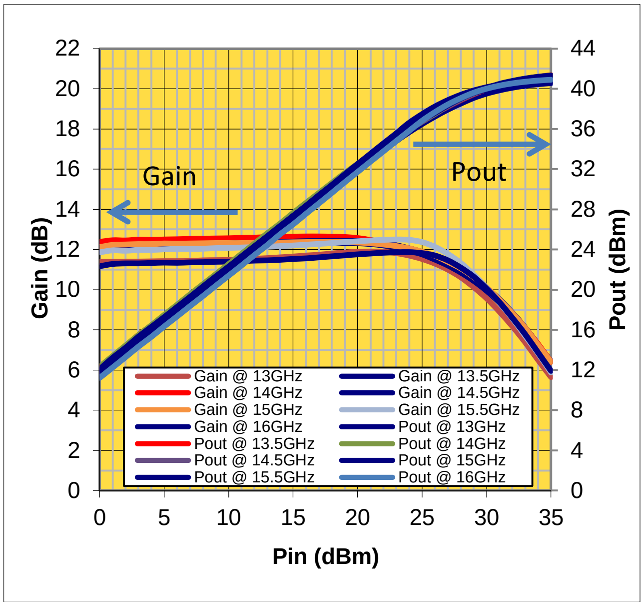
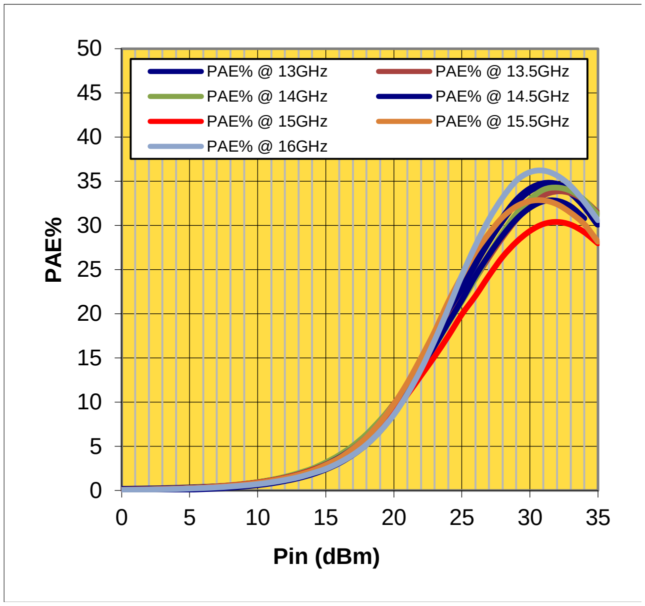


Measured fixture Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. **

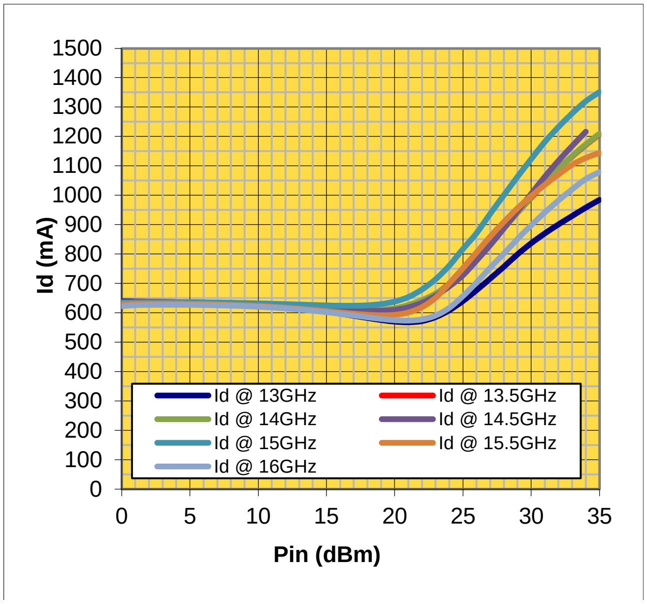
GAIN, Pout vs. Pin



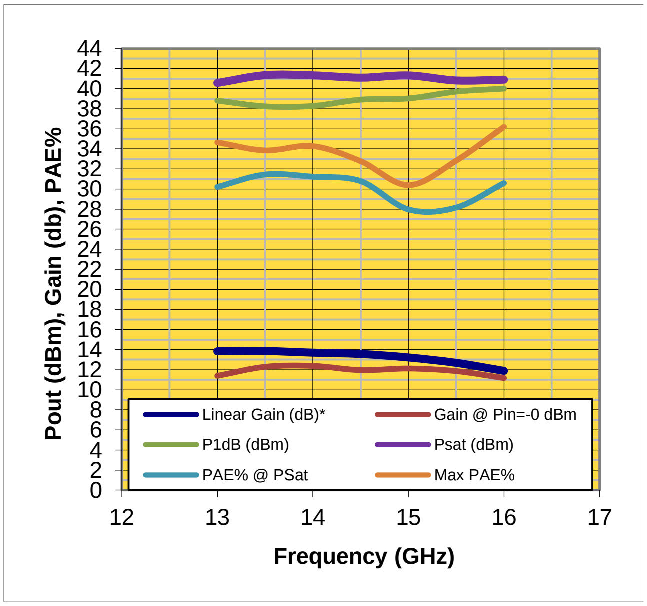
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



**CW Fixture *On-wafer Pulsed Power

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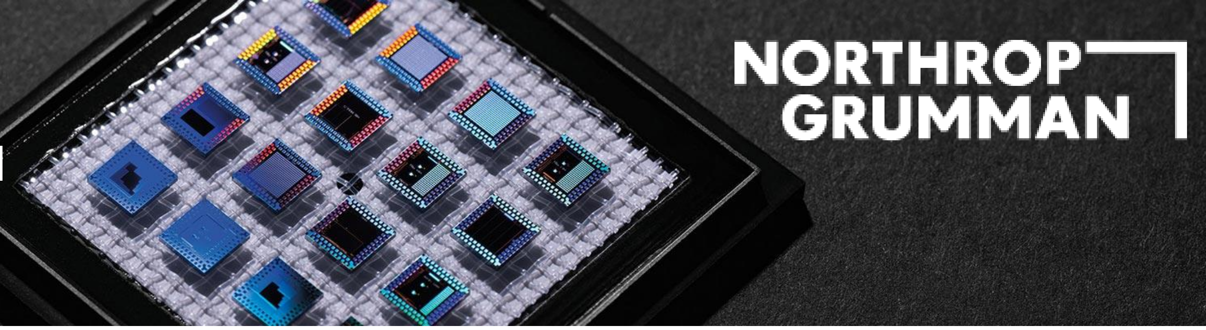

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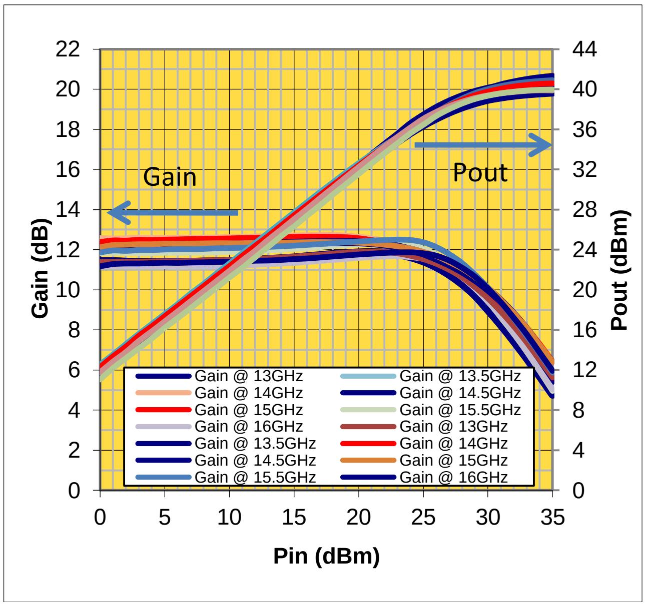
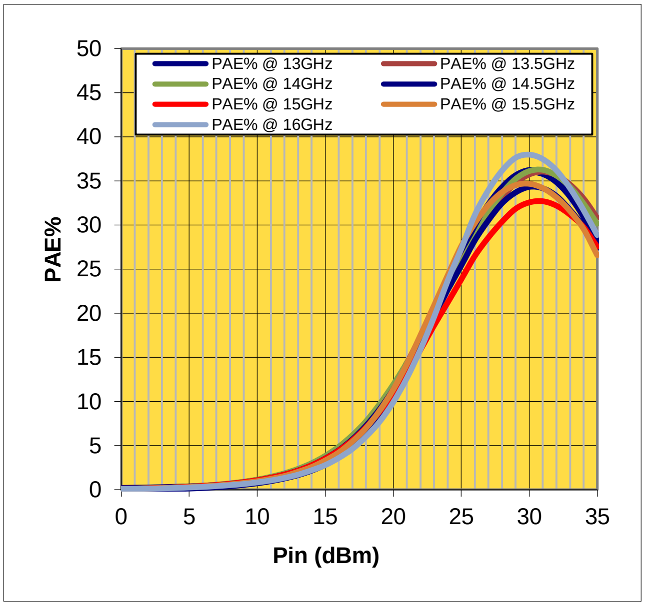
Measured fixture Performance Characteristics (Typical Performance at 25°C)
Vd = 24 V, Id = 640 mA. **

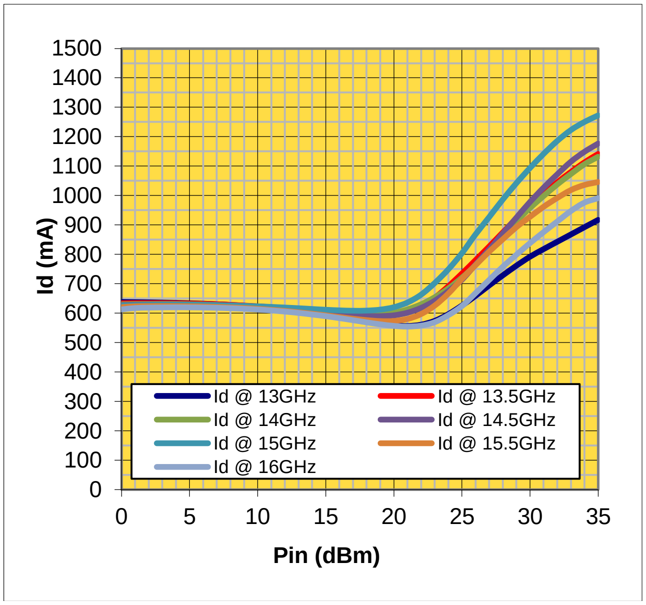
GAIN, Pout vs. Pin



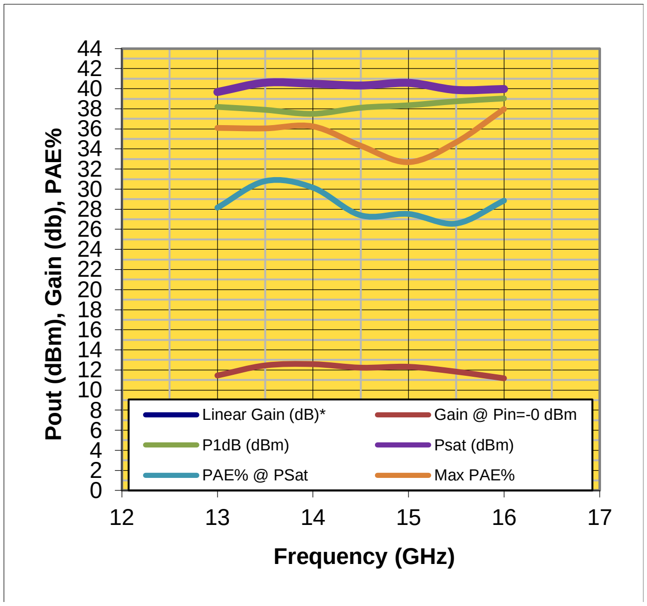
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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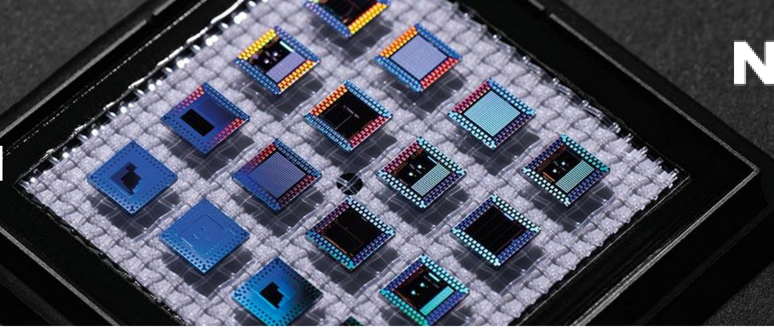

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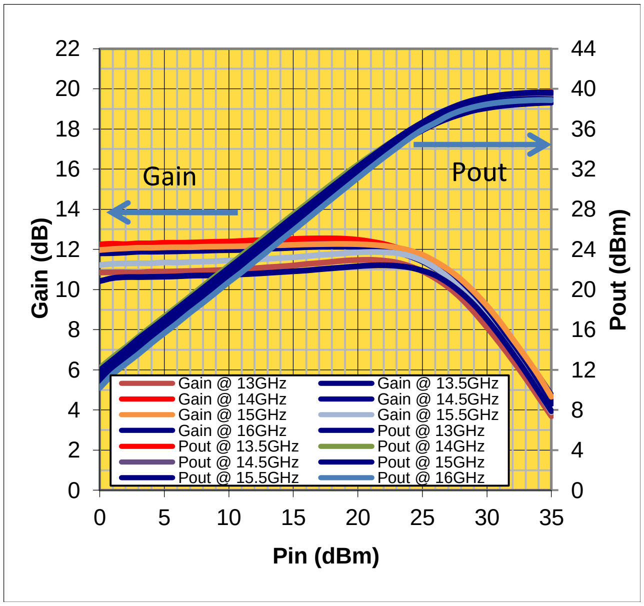
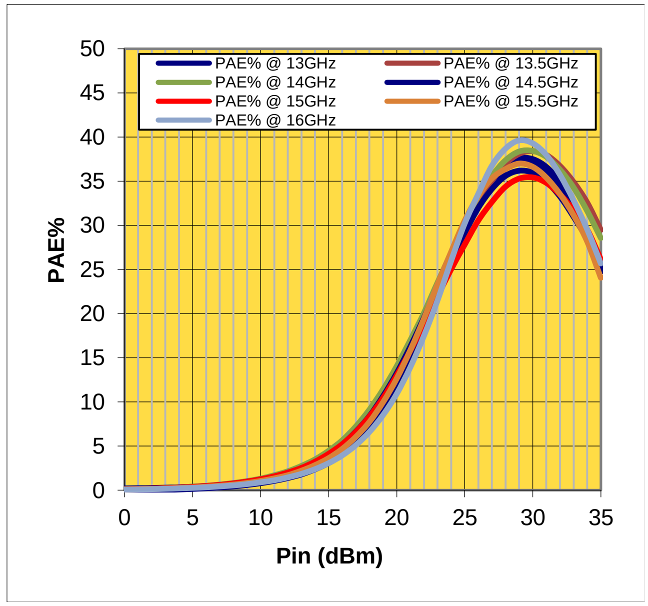
Measured fixture Performance Characteristics (Typical Performance at 25°C)
Vd = 20 V, Id = 640 mA. **

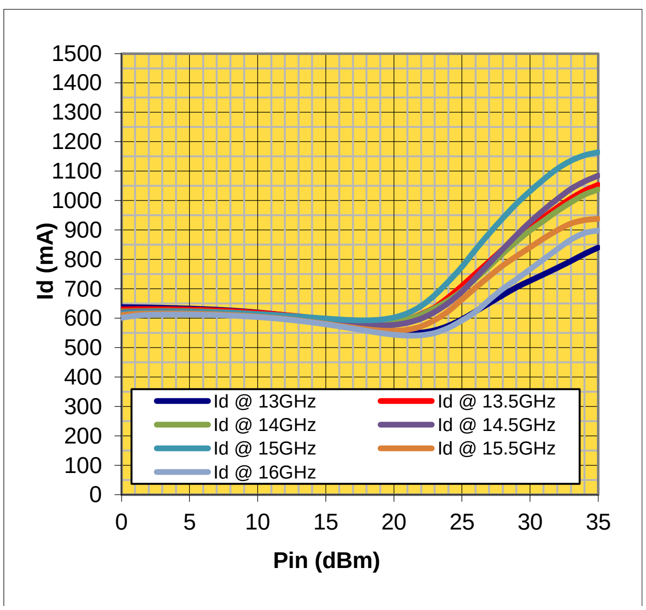
GAIN, Pout vs. Pin



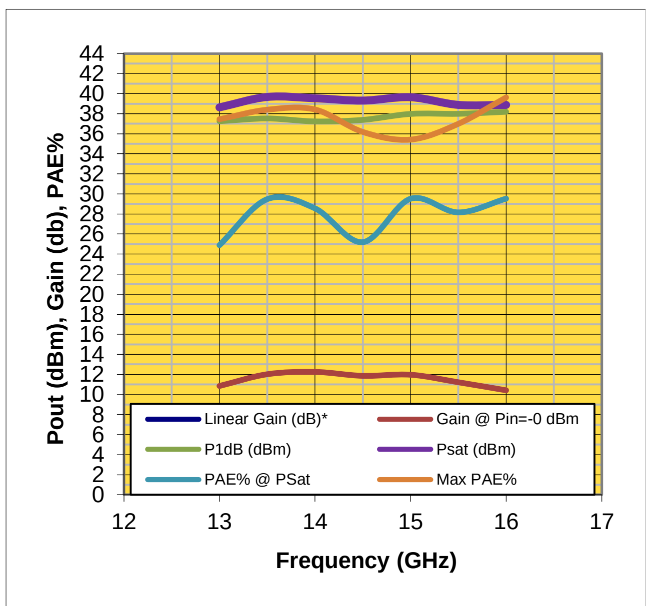
PAE vs. Pin



Id vs Pin



Pout, Gain, PAE vs. Frequency



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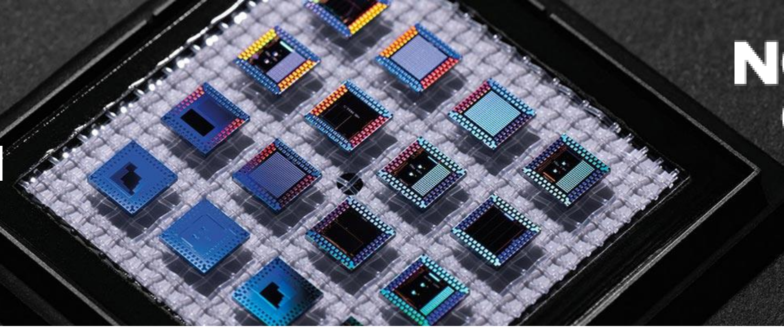

On-wafer measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28 V, Id = 640 mA. (single channel) *

Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
8.0	0.763	-118.728	2.025	-5.316	0.026	-79.725	0.643	105.703
8.5	0.745	-129.232	2.475	-29.249	0.035	-109.207	0.581	90.176
9.0	0.727	-144.920	3.063	-54.848	0.049	-135.564	0.500	68.623
9.5	0.660	-165.250	3.844	-84.234	0.064	-159.157	0.401	33.060
10.0	0.551	168.079	4.640	-117.414	0.077	167.180	0.369	-26.017
10.5	0.338	132.231	5.184	-155.335	0.087	129.682	0.442	-89.481
11.0	0.173	88.903	5.221	167.878	0.100	94.397	0.570	-135.864
11.5	0.109	-2.669	4.972	134.073	0.099	61.580	0.639	-168.949
12.0	0.121	-42.153	4.772	103.029	0.096	33.347	0.634	164.069
12.5	0.190	-67.395	4.772	72.213	0.099	3.157	0.593	137.031
13.0	0.206	-92.413	4.877	37.631	0.107	-31.666	0.503	105.027
13.5	0.183	-137.289	4.978	-2.741	0.109	-69.653	0.408	53.102
14.0	0.184	101.705	4.581	-51.124	0.102	-119.302	0.481	-25.051
14.5	0.464	23.429	3.251	-102.034	0.075	-165.984	0.694	-86.861
15.0	0.687	-19.644	1.868	-141.891	0.042	158.450	0.830	-122.949
15.5	0.790	-45.634	1.067	-169.984	0.023	125.612	0.895	-146.686
16.0	0.868	-66.251	0.636	166.489	0.014	93.154	0.921	-162.925
16.5	0.883	-80.739	0.398	148.501	0.007	63.953	0.942	-174.306
17.0	0.913	-94.134	0.258	133.907	0.006	77.989	0.957	175.897
17.5	0.898	-103.079	0.175	117.097	0.004	60.761	0.974	166.982
18.0	0.943	-113.030	0.121	102.141	0.003	48.952	0.979	158.426
18.5	0.919	-120.648	0.082	92.753	0.003	23.430	0.972	149.970
19.0	0.959	-129.866	0.062	79.009	0.005	29.283	0.959	141.554
19.5	0.945	-137.015	0.053	66.885	0.004	31.623	0.950	131.493
20.0	0.969	-144.637	0.043	48.927	0.001	66.212	0.895	117.360
20.5	0.948	-152.423	0.038	17.435	0.001	129.984	0.553	82.893
21.0	0.969	-158.197	0.020	-28.627	0.001	-106.560	0.280	177.907
21.5	0.921	-166.413	0.005	-35.339	0.003	33.807	0.820	158.926
22.0	0.961	-170.156	0.004	12.052	0.004	-135.315	0.939	142.715
22.5	0.906	-177.330	0.005	18.547	0.004	-78.396	0.959	131.501
23.0	0.969	178.450	0.003	-6.674	0.004	3.125	0.974	123.035
23.5	0.924	171.476	0.002	25.446	0.003	146.767	0.964	116.072
24.0	0.978	166.907	0.004	8.586	0.007	1.366	0.965	110.042

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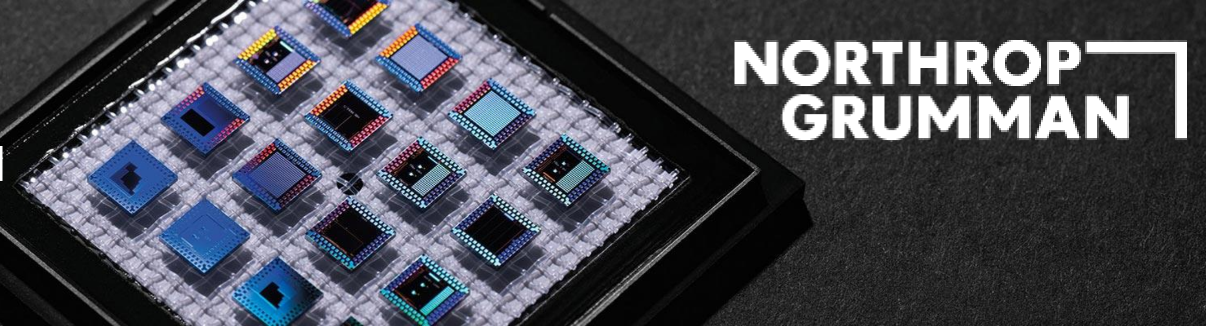
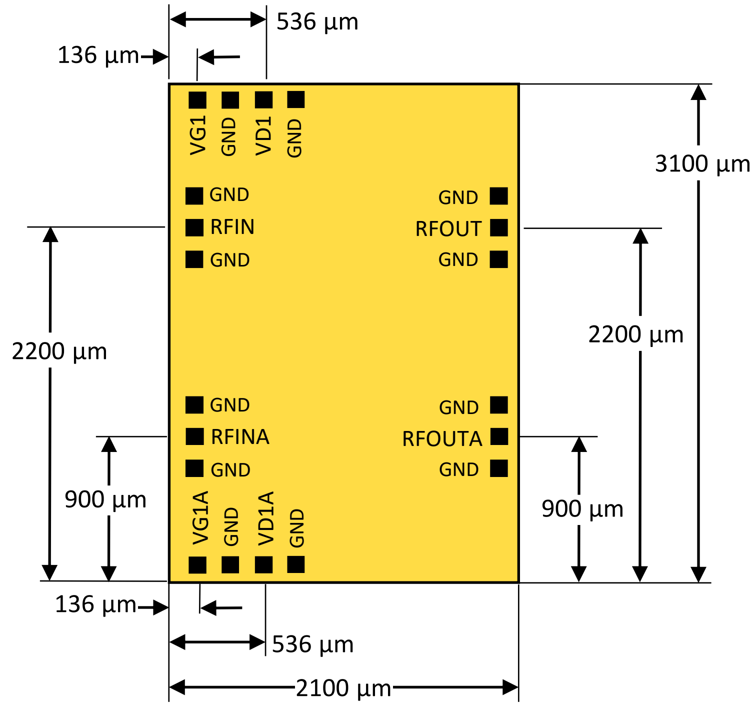


Die Size and Bond Pad Locations (Not to Scale)

X = 2100 ± 25 µm
Y = 3100 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

APN237 should be biased from the top and bottom of the die. For best performance each side should be biased up separately, but they can be tied together.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
   i. Apply negative gate voltage (-5 V) to ensure that all devices are off
   ii. Ramp up drain bias to ~10 V
   iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
   iv. Ramp up drain to operating bias
   v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
   i. Gradually decrease drain bias to 0 V.
   ii. Gradually decrease gate bias to 0 V.
   iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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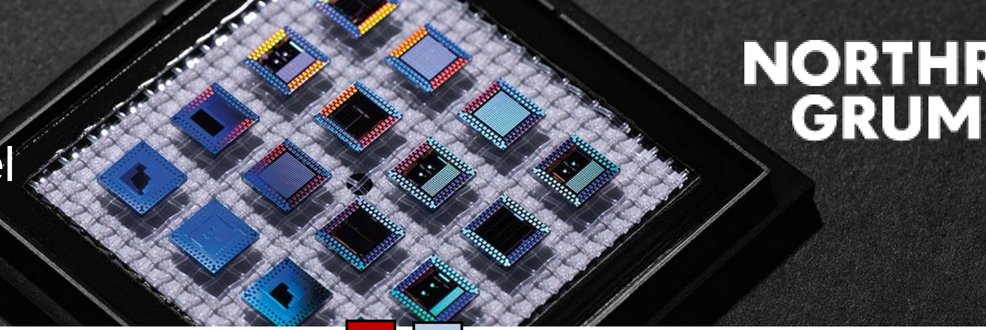
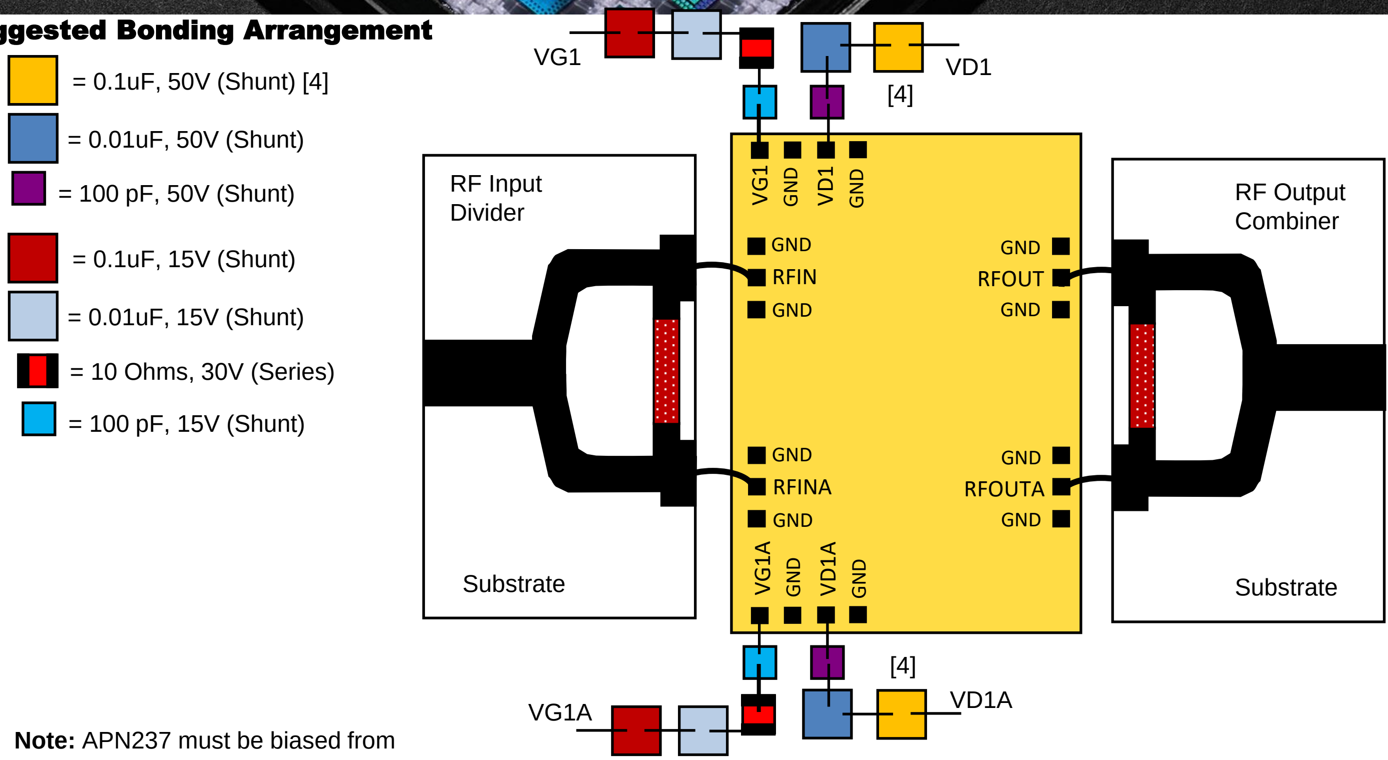


Suggested Bonding Arrangement



Note: APN237 must be biased from the top and bottom bias pads.

Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most Northrop Grumman Aerospace Systems (NGAS) GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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