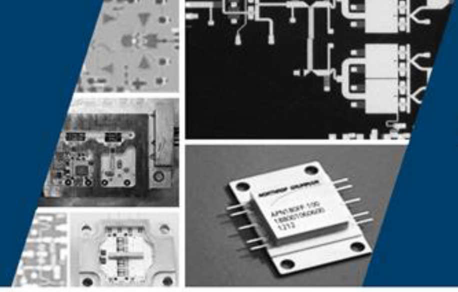
APN243
24-28 GHz
GaN Power Amplifier



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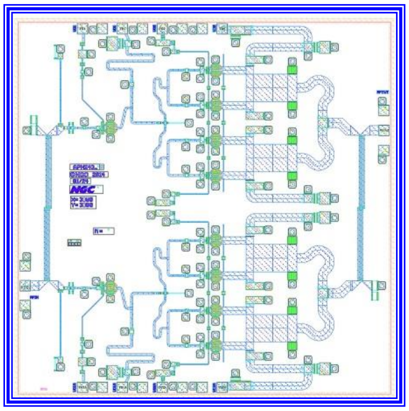
Advance Datasheet

Revision: May 2016



X = 3.8mm Y = 3.8mm

Product Features

- RF frequency: 24 to 28 GHz
- Linear Gain: 20 dB typ.
- Psat: 40.5 dBm typ.
- Die Size: 14.44 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1.0 A

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- Space-Earth Communications
- Space Research & Earth Exploration

Product Description

The APN243 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Ka-Band communication applications such as point-to-point and point-to-multipoint digital (LMDS) radios and SatCom Terminals. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification *	Min	Typ	Max	Unit
Frequency	24		28	GHz
Linear Gain	18	20		dB
Input Return Loss	18	20		dB
Output Return Loss	15	20		dB
P1db (PP*)		38		dBm
Psat (PP*)	39.5	40.5		dBm
PAE @ Psat (PP*)		27		%
Max PAE (PP*)		29.5		%
Vd1=Vg1a, Vd2=Vd2a		28		V
Vg1. Vg1a		-3.5		V
Vg2, Vg2a		-3.5		V
Id1+Id1a		200		mA
Id2+Id2a		800		mA

* Pulsed-Power On-Wafer unless otherwise noted

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1=Vg1a ,Vd2=Vd2a	20	28	V
Id1+Id1a		240	mA
Id2+Id2a		960	mA
Vg1, Vg1a, Vg2, Vg2a	-5	0	V
Input drive level		TBD	dBm
Assy. Temperature (TBD seconds)		300	deg. C

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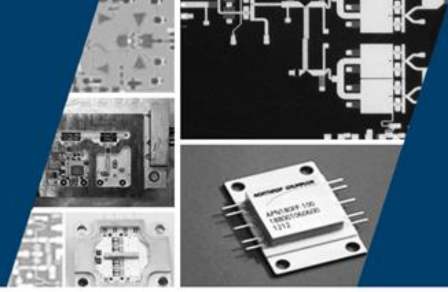
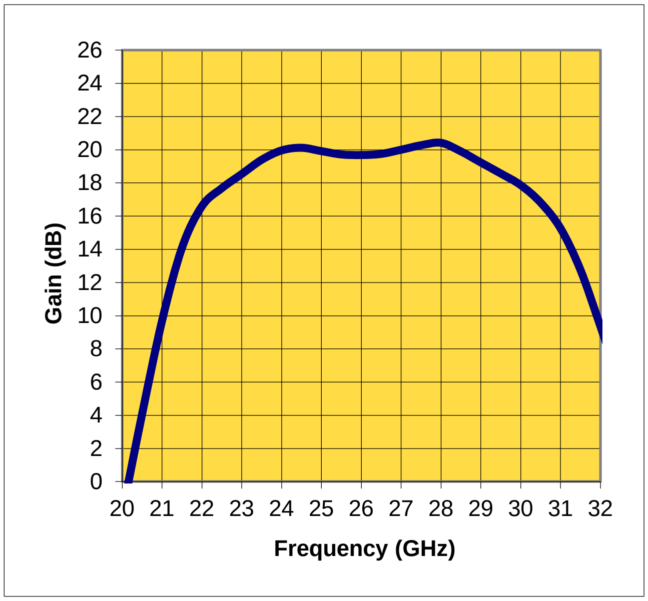
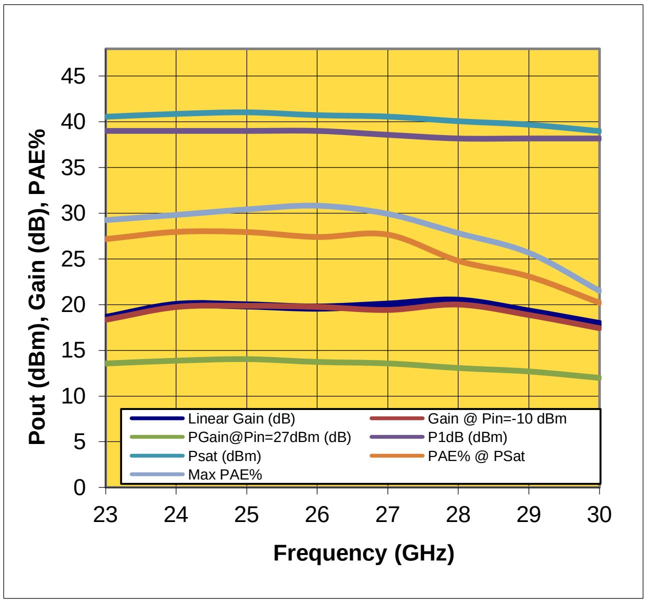


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 200 mA, Id2 + Id2a = 800 mA

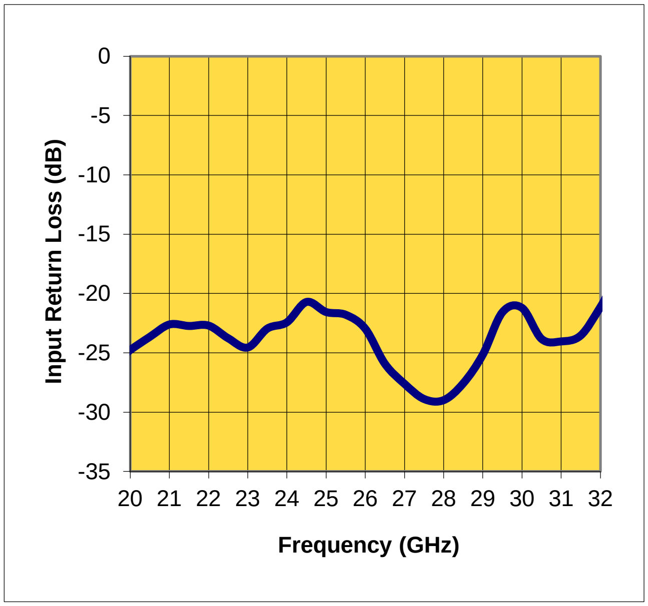
Linear Gain vs. Frequency *



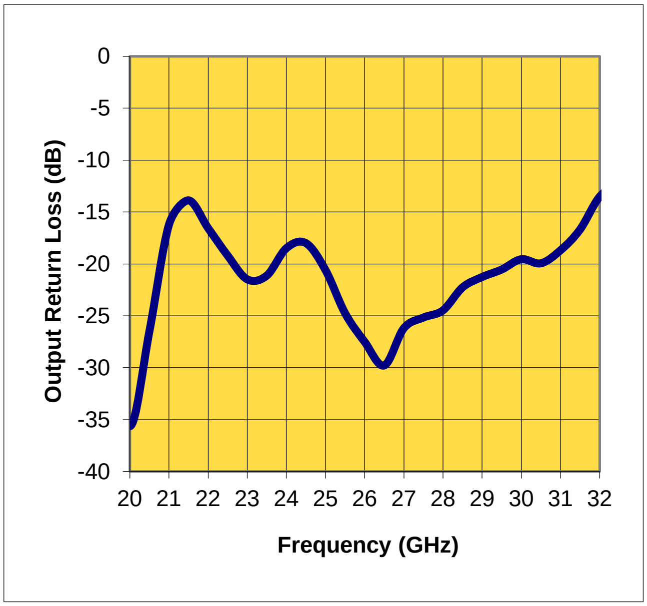
Power, Gain, PAE% vs. Frequency *



Input Return Loss vs. Frequency *



Output Return Loss vs. Frequency *



* Pulsed-Power On-Wafer

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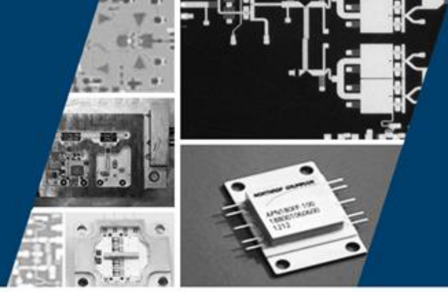

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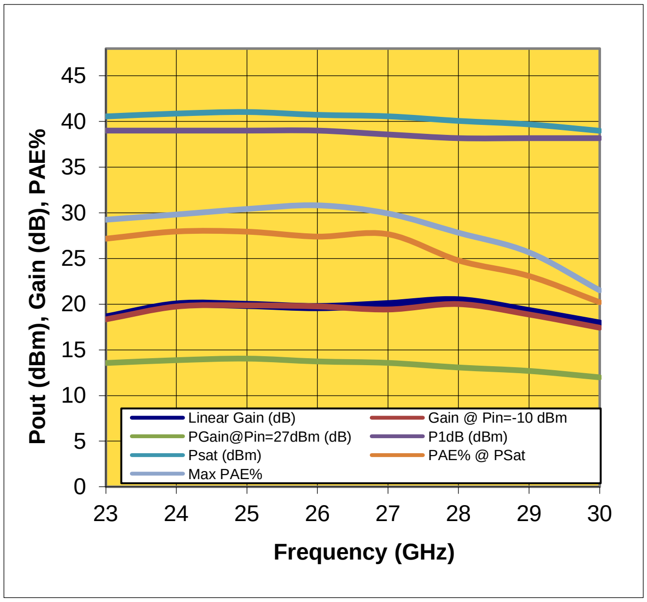
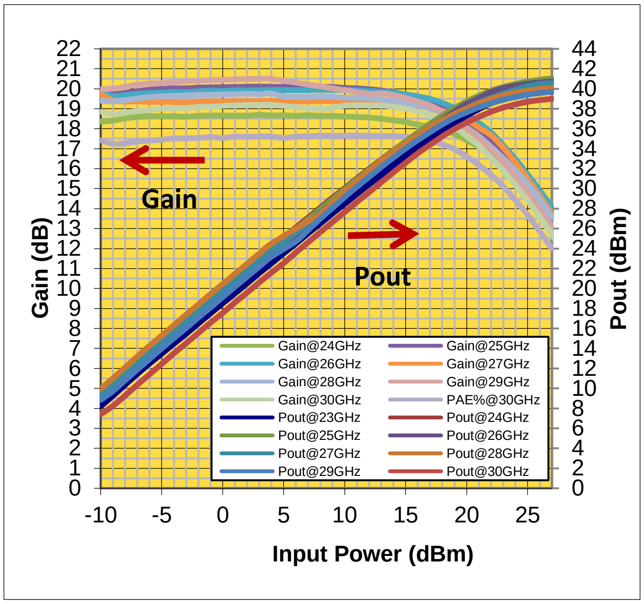
Measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1 + Id1a = 200 mA, Id2 + Id2a = 800 mA

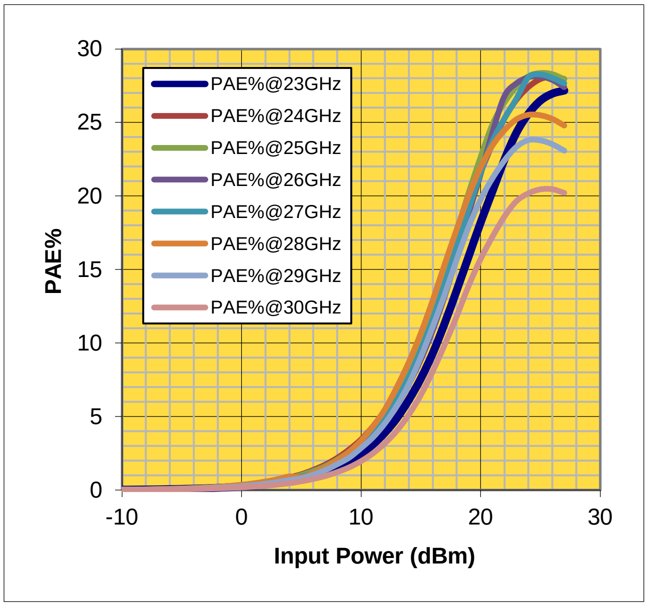
Power, Gain, PAE% vs. Frequency Pulsed-Power On-Wafer



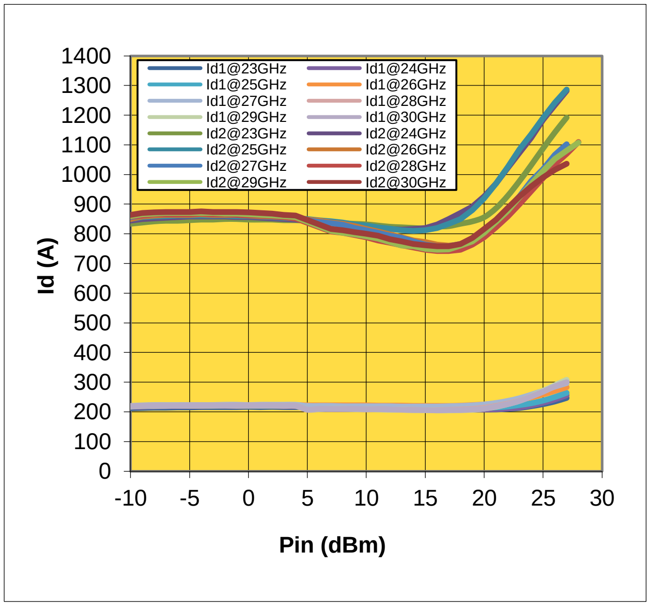
Output Power, Gain vs. Input Power Pulsed-Power On-Wafer

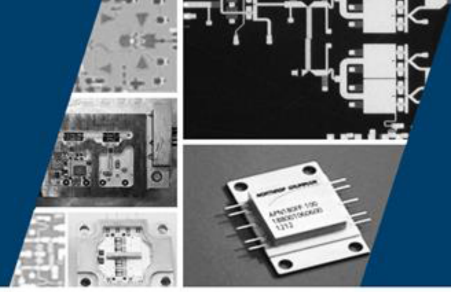


PAE% vs. Input Power Pulsed-Power On-Wafer



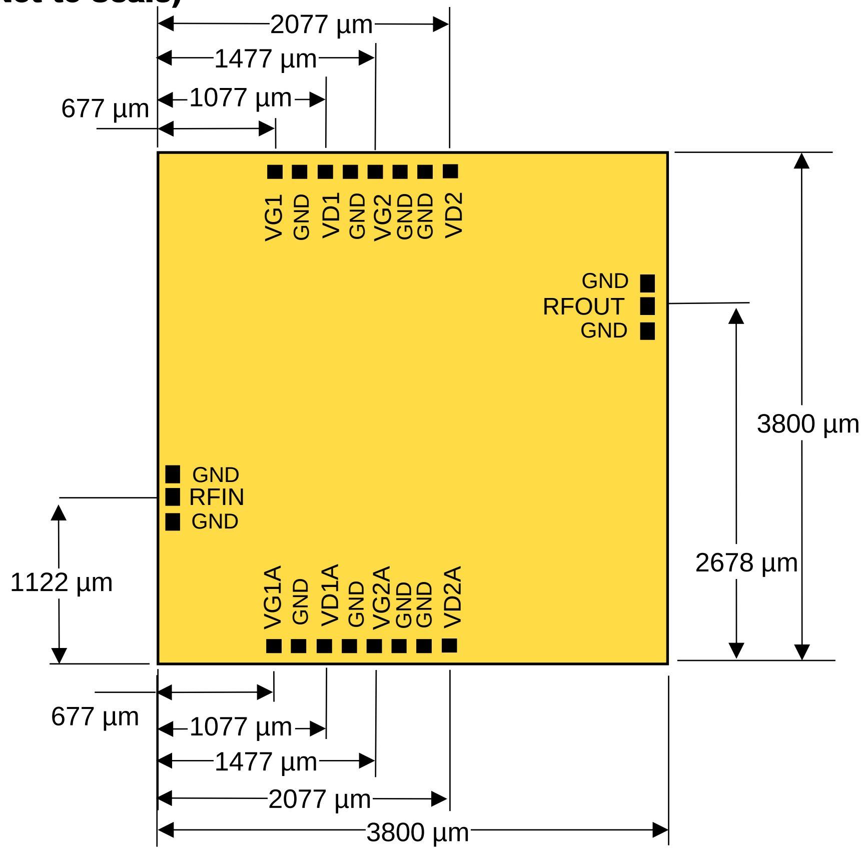
Stage Currents vs. Input Power Pulsed-Power On-Wafer





Die Size and Bond Pad Locations (Not to Scale)

X = 3800 µm ± 25 µm
Y = 3800 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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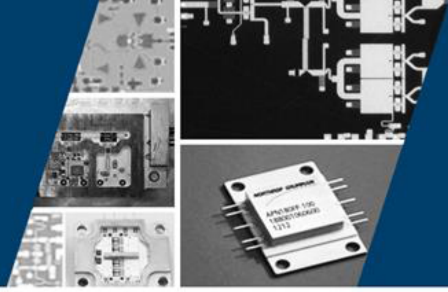
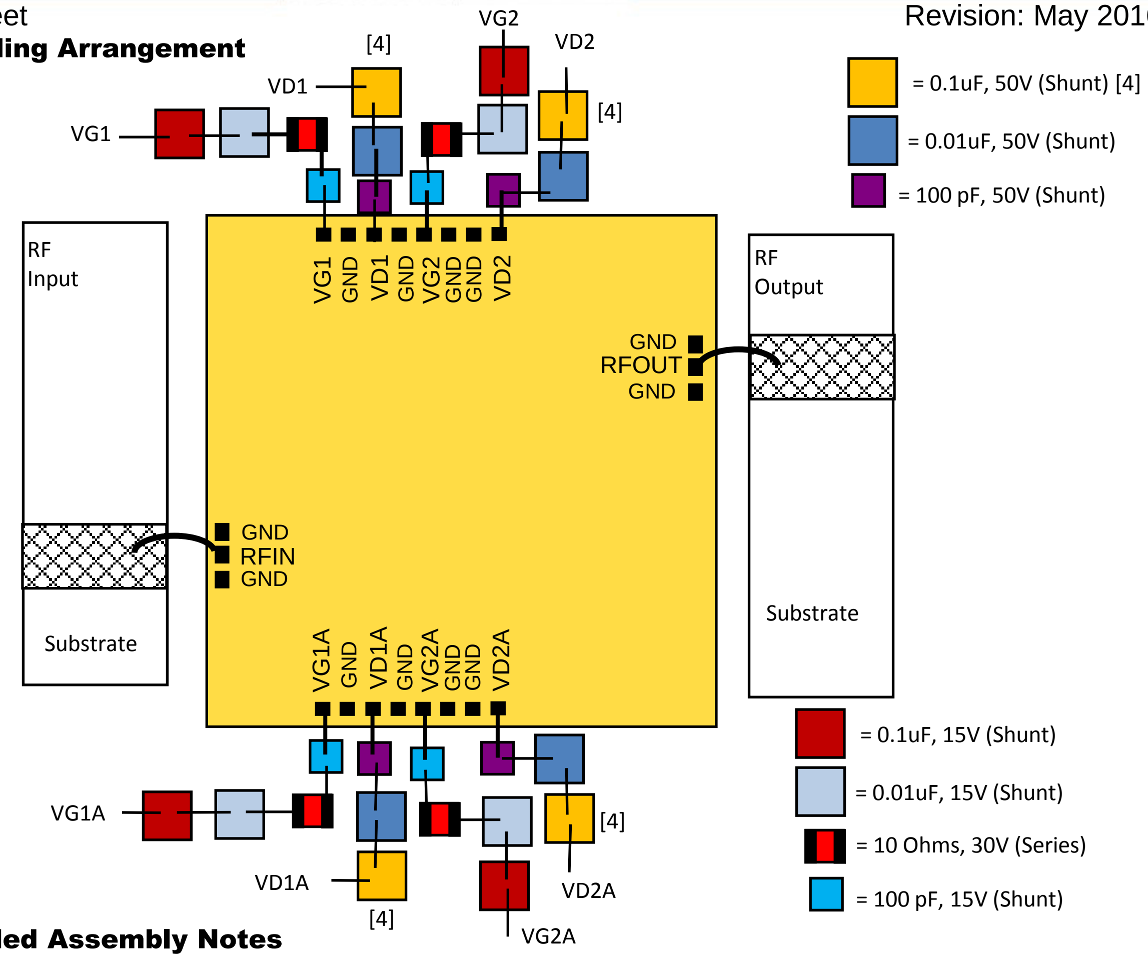


Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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