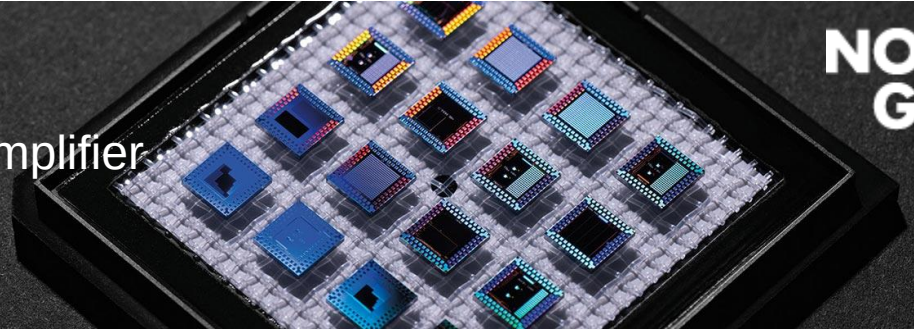
APN311
27 – 31 GHz
GaN Power Amplifier



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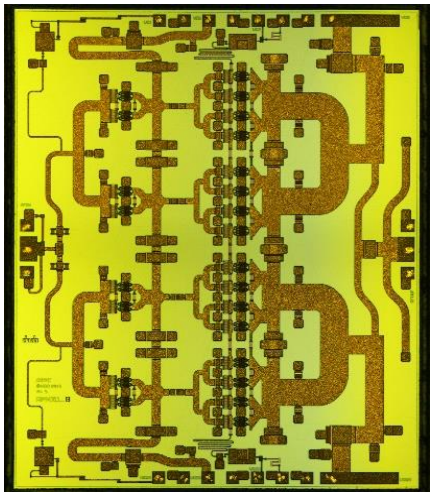

x=3.30mm; y=4.10 mm

Product Features

- RF frequency: 27 to 31 GHz
- Linear Gain: 20 dB typ.
- Psat: 45.6 dBm typ.
- Die Size: 13.52 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 2.64 A

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

Product Description

The APN311 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in Ka-Band communication applications such as SatCom Terminals and point-to-point and point-to-multipoint digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Performance Characteristics (Ta = 25°C)

Specification *	Min	Typ	Max	Unit
Frequency	27		31	GHz
Linear Gain	19	20		dB
Input Return Loss	5	12		dB
Output Return Loss	>5	10		dB
P1db (PP*)		43		dBm
Psat (PP*)	44	45		dBm
PAE @ Psat (PP*)		30		%
Max PAE (PP*)	30			%
Vd1=Vg1a, Vd2=Vd2a	20		28	V
Vg1. Vg1a		-3.56		V
Vg2, Vg2a		-3.46		V
Id1+Id1a		830		mA
Id2+Id2a		1860		mA

* Pulsed-Power On-Wafer unless otherwise noted

Export Information
ECCN: **5A991.g**
HTS (Schedule B) code: **8542.33.0000**

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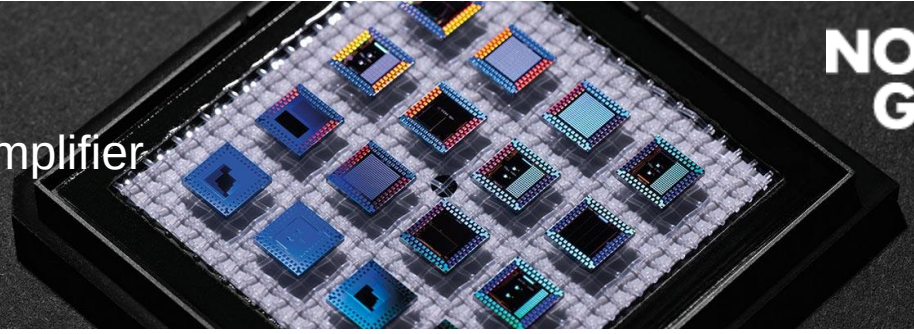

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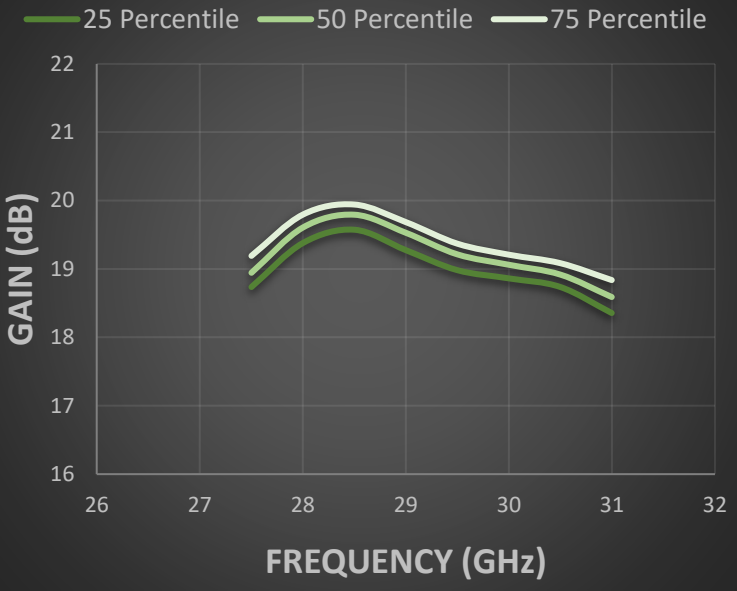
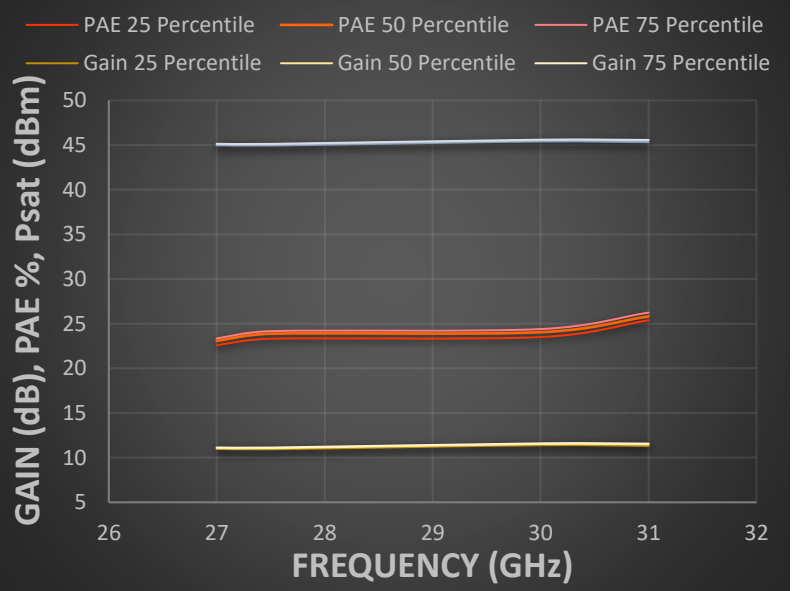
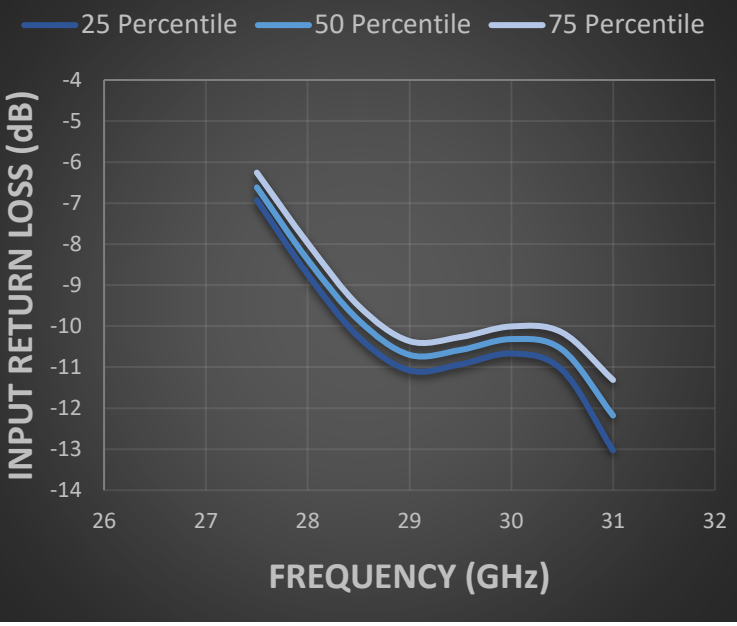
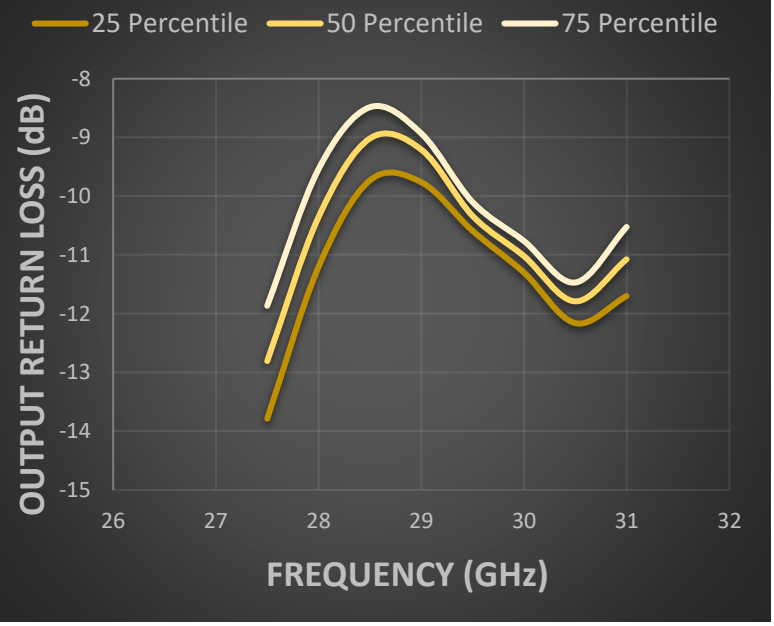
On Wafer Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 830 mA, Id2 + Id2a = 1860 mA









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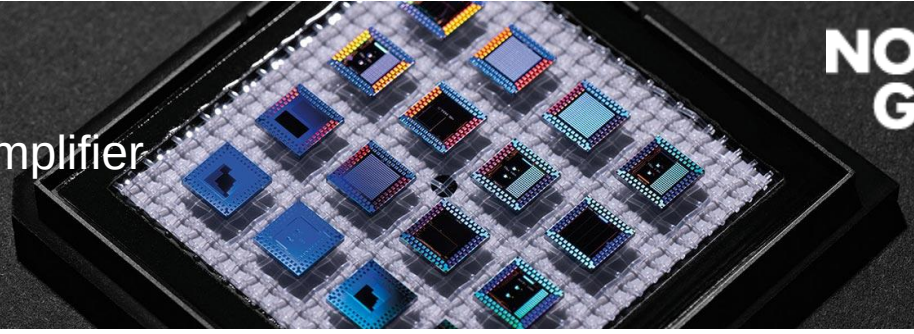

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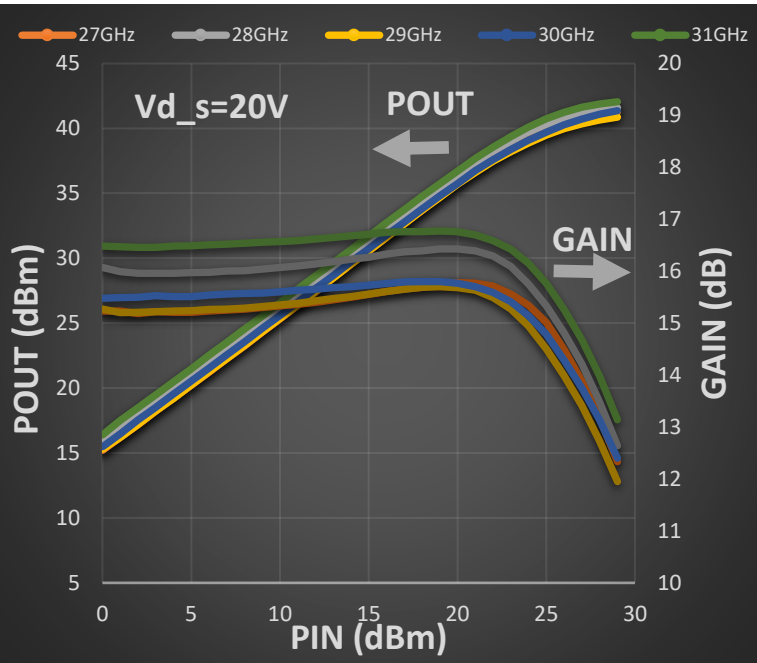
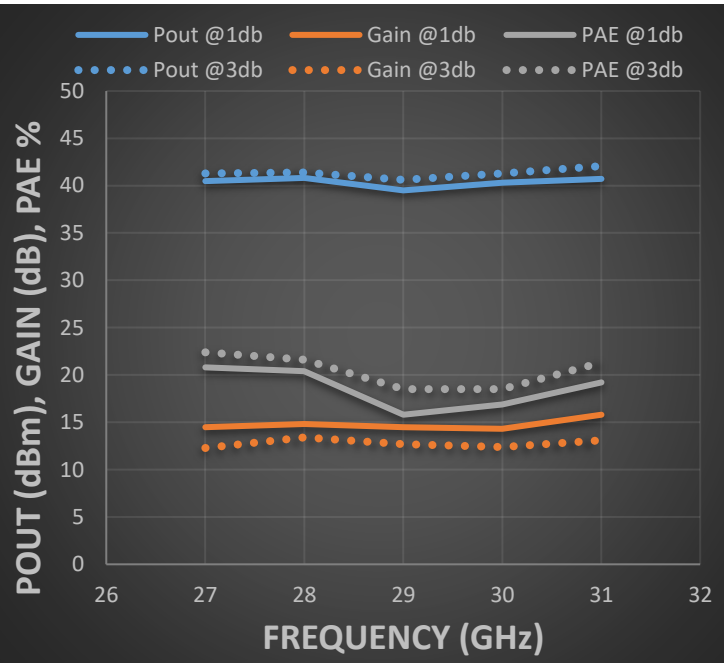
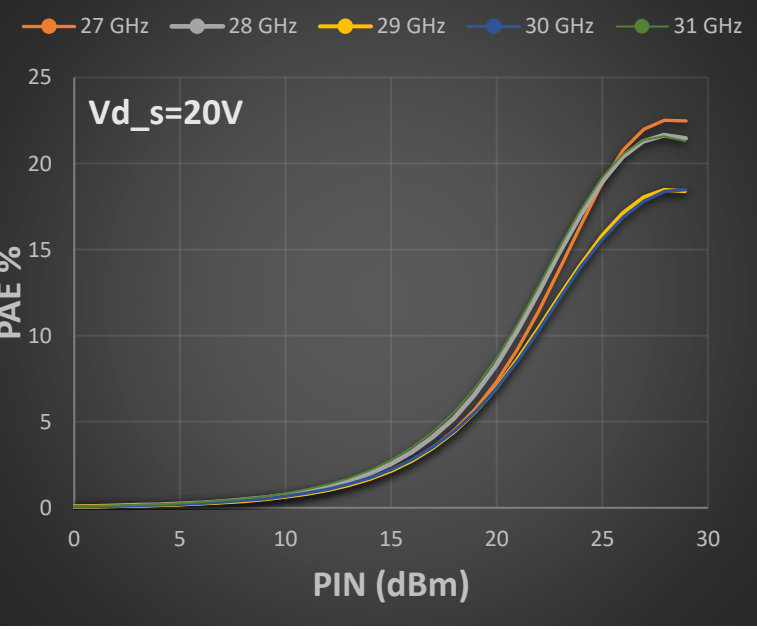
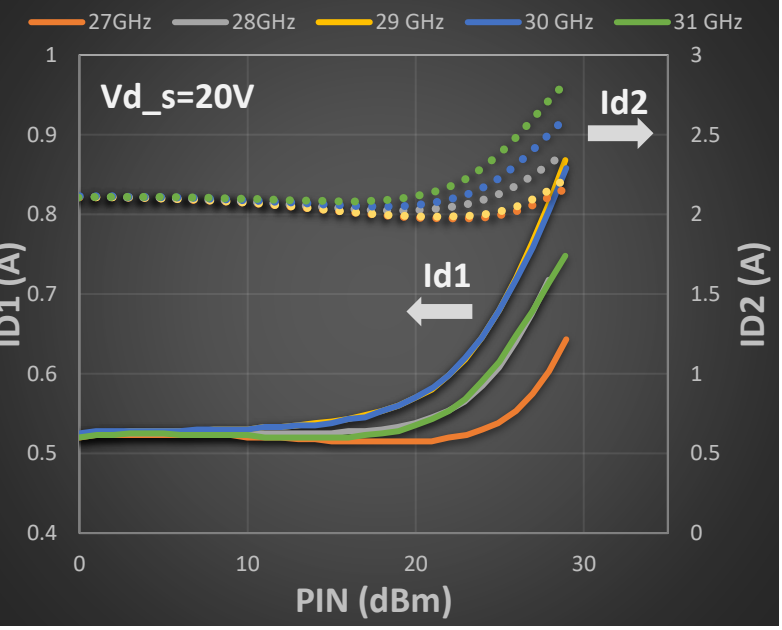
Fixture Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 20.0 V, Id1 + Id1a = 830 mA, Id2 + Id2a = 1860 mA









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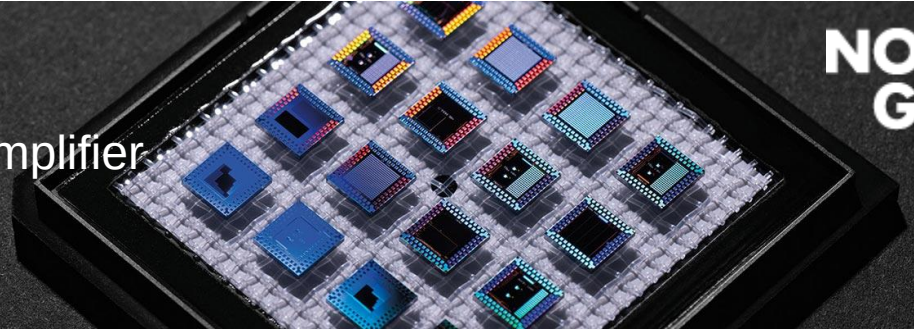

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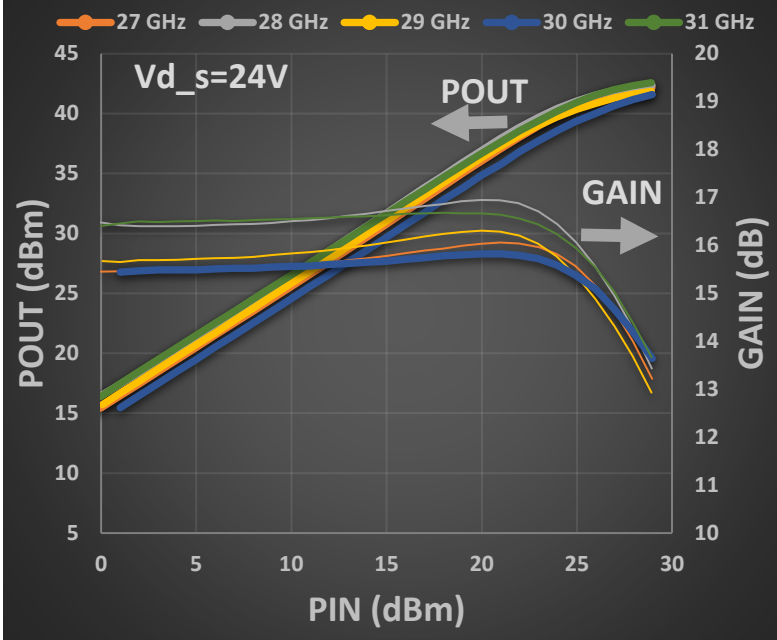
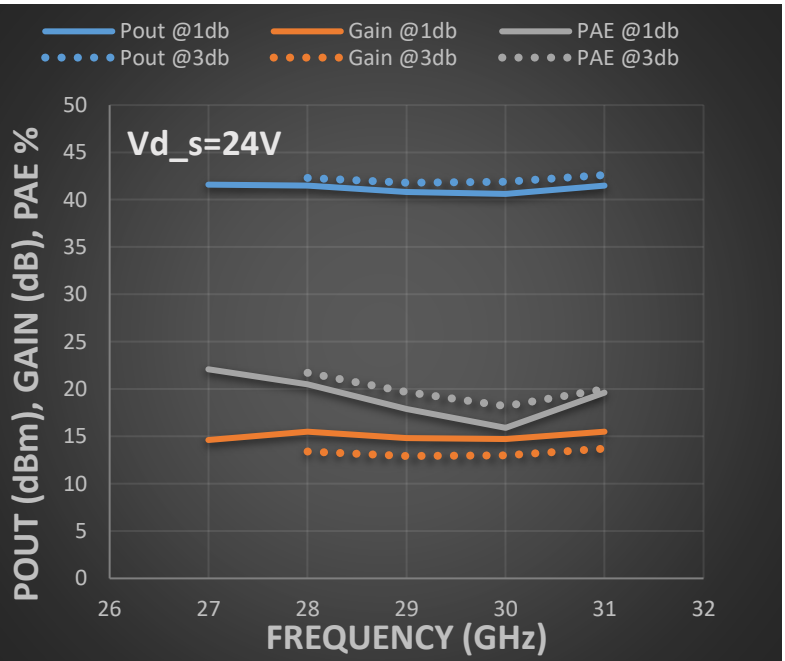
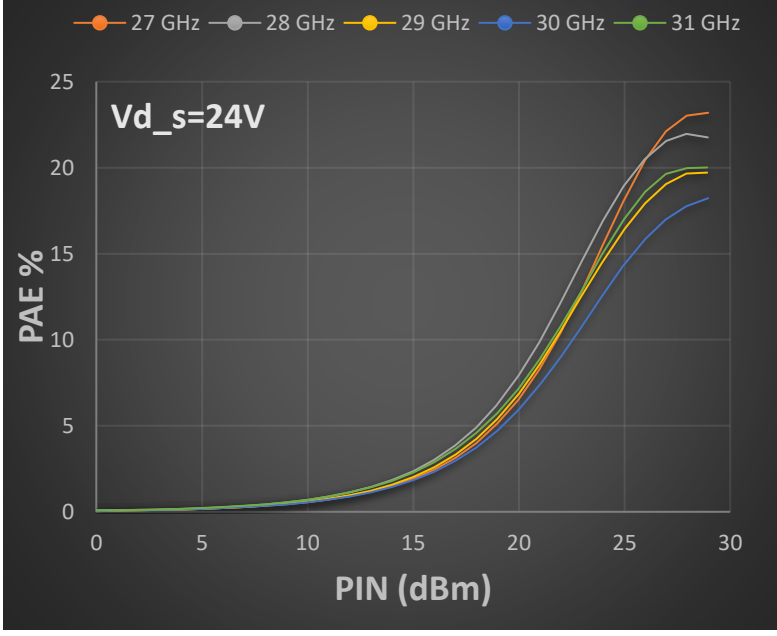
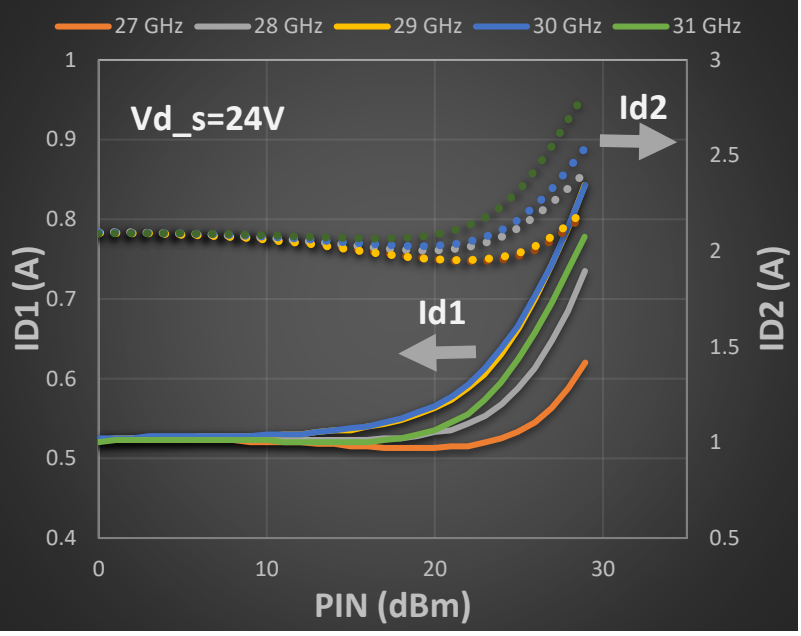
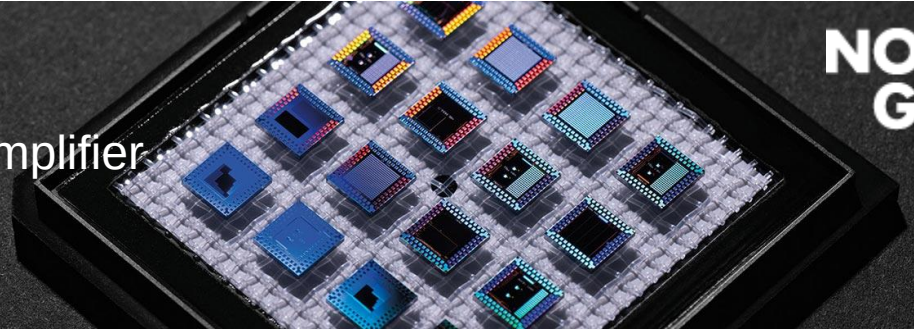
Fixture Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 24.0 V, Id1 + Id1a = 830 mA, Id2 + Id2a = 1860 mA











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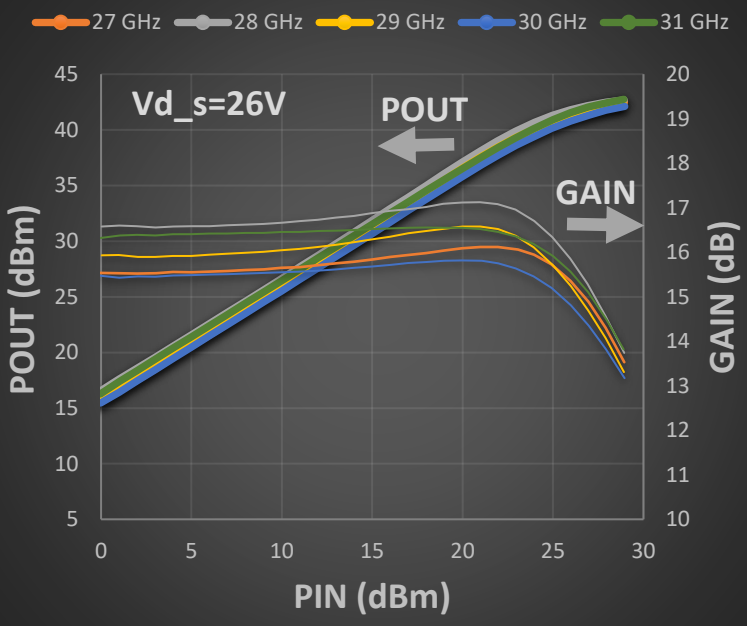
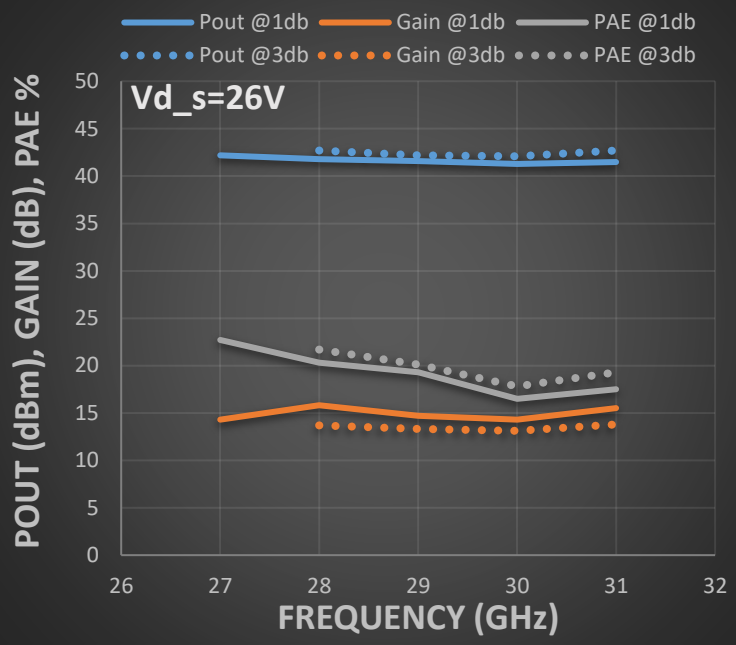
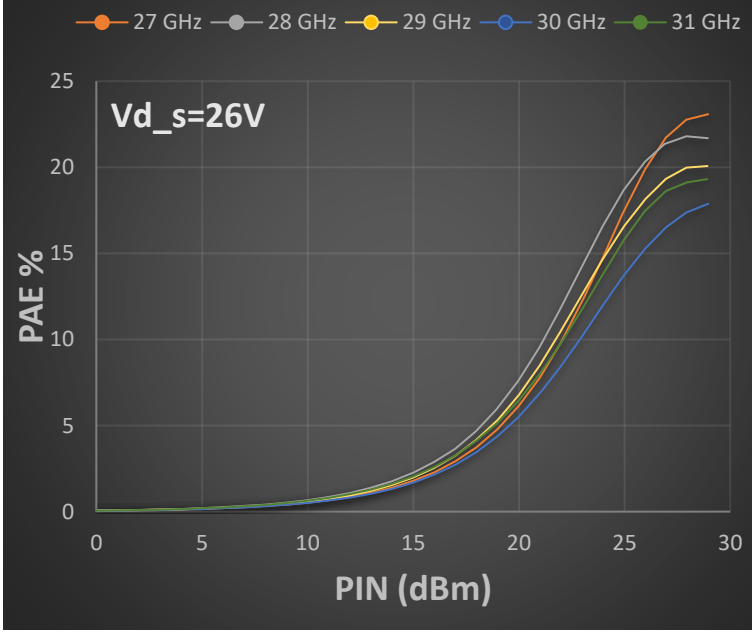
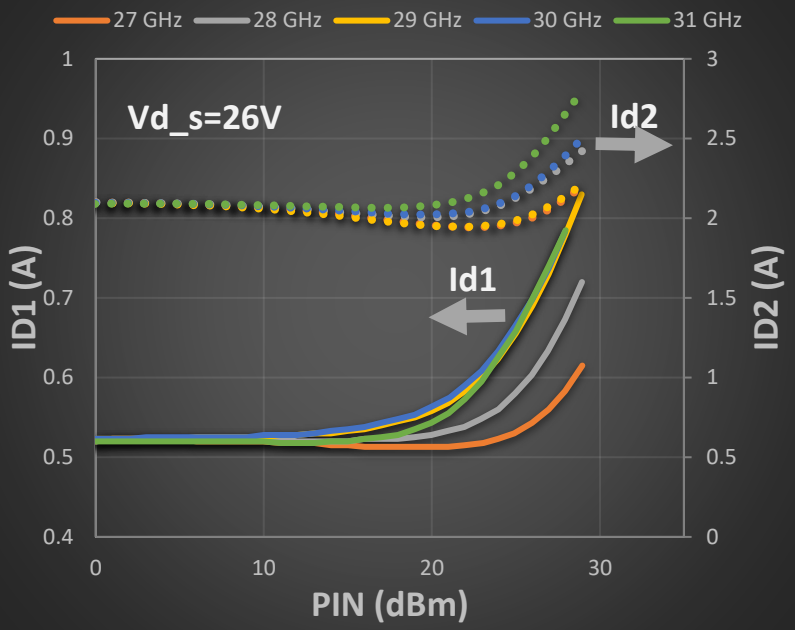
Fixture Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 26.0 V, Id1 + Id1a = 830 mA, Id2 + Id2a = 1860 mA









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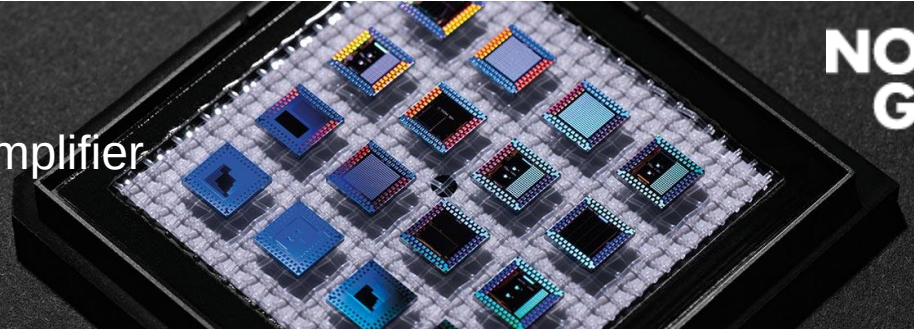

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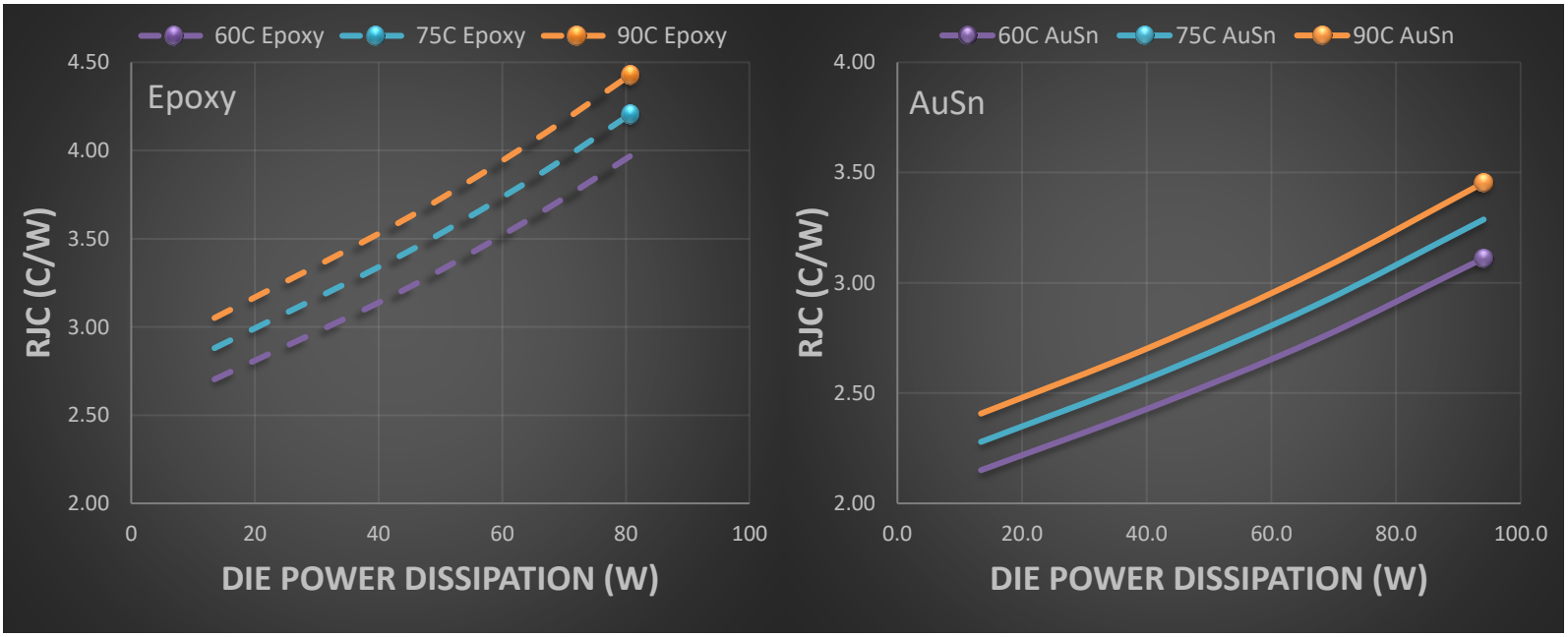
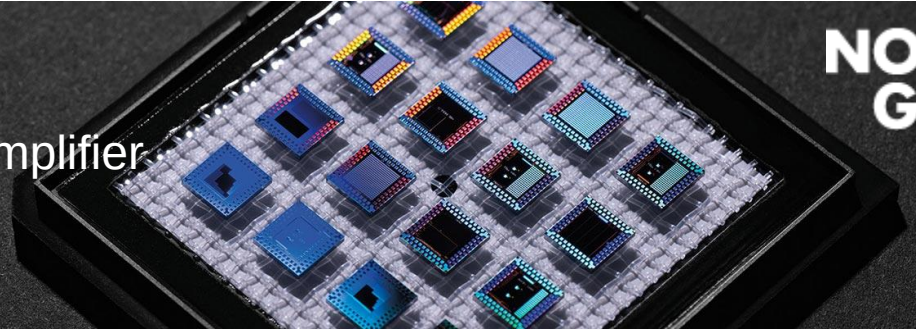
Thermal Properties

Preliminary Thermal Properties with die mounted with 30um 80/20 AuSn Eutectic* to: 25mil CuW85 Shim.

Shim	Mounting Material	Shim Boundary Temperature	Junction Temperature Tjc	Power Dissipation (W)	Thermal Resistance Rjc (°C/W)
25 mil CuW	AuSn Eutecic	60 °C	89	13.4	2.15
			158	40.3	2.43
			244	67.2	2.74
			353	94.1	3.11
		75 °C	106	13.4	2.28
			179	40.3	2.57
			270	67.2	2.90
			384	94.1	3.29
		90 °C	122	13.4	2.41
			199	40.3	2.71
			295	67.2	3.05
			415	94.1	3.45
25 mil CuW	965 Epoxy	60 °C	96	13.4	2.70
			187	40.3	3.14
			243	53.8	3.40
			307	67.2	3.67
		75 °C	114	13.4	2.88
			210	40.3	3.35
			269	53.8	3.61
			336	67.2	3.89
		90 °C	131	13.4	3.05
			233	40.3	3.54
			295	53.8	3.81
			366	67.2	4.11



* Assumed thermal conductivity of 57 W/m/K
** Vd = 28.0 V, Idq1 = 830 mA, Id2q = 1860 mA
*** Max recommended. Pre-qualification reliability testing indicates that MTTF in excess of 10^6 hours can be achieved by ensuring Tjc is kept below 200ºC.



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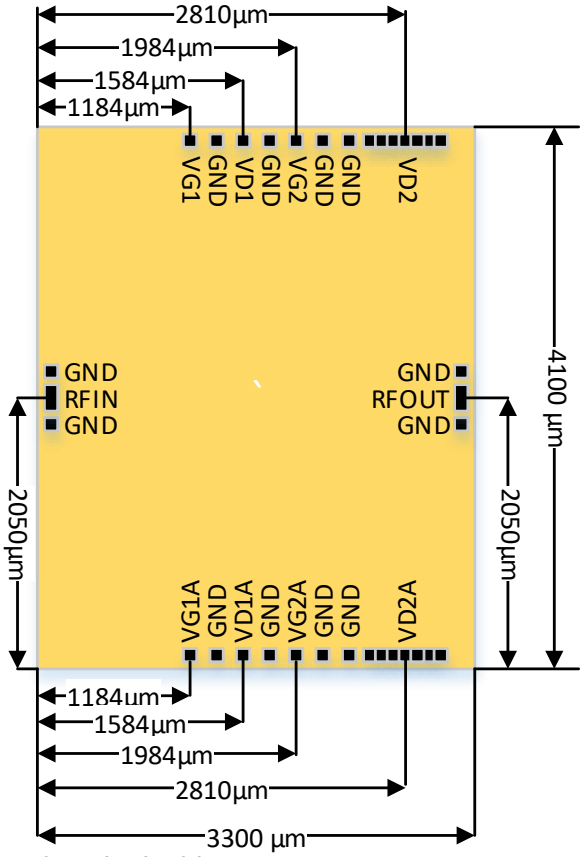
Die Size and Bond Pad Locations (Not to Scale)

X = 3300 µm ± 25 µm
Y = 4100 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-8 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by de-biasing output amplifier stages first (if applicable):
    i. Set gate voltage back to pinch-off (-8V).
    ii. Gradually decrease drain bias to 0 V.
    iii. Gradually decrease gate bias to 0 V.
    iv. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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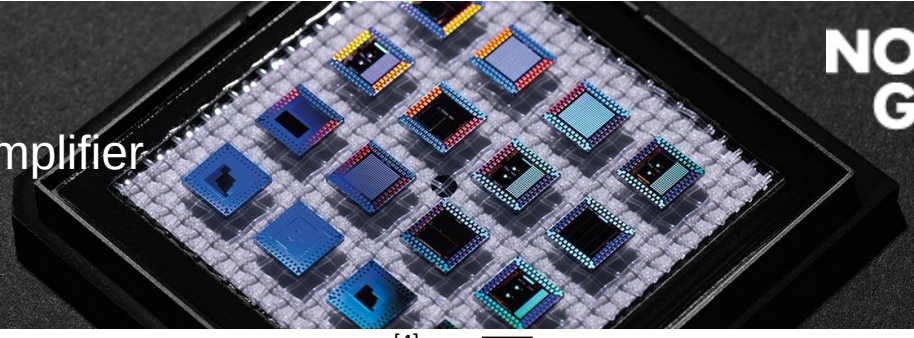

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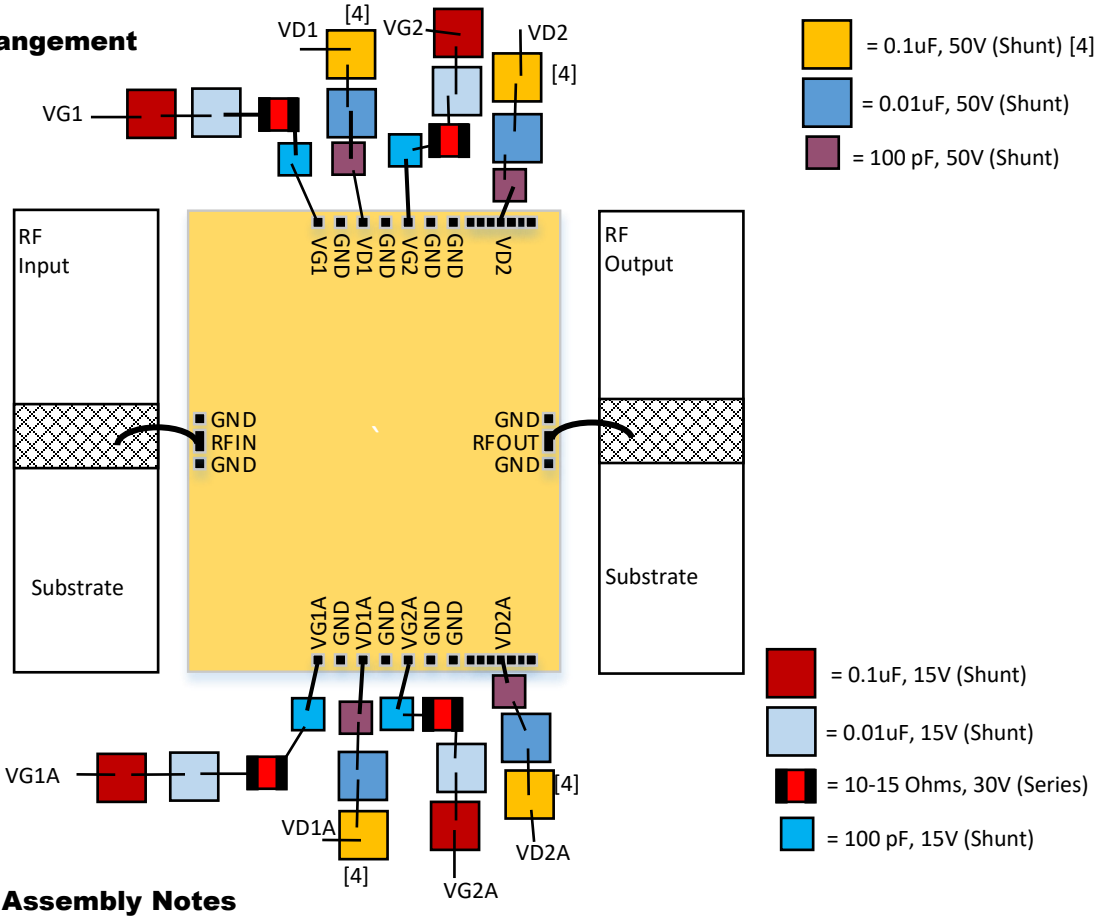
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGSS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGSS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320°C for 30 seconds.

Note: Many of the NGSS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!

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Approved for Public Release: Northrop Grumman Case 20-1836, 9/14/2020