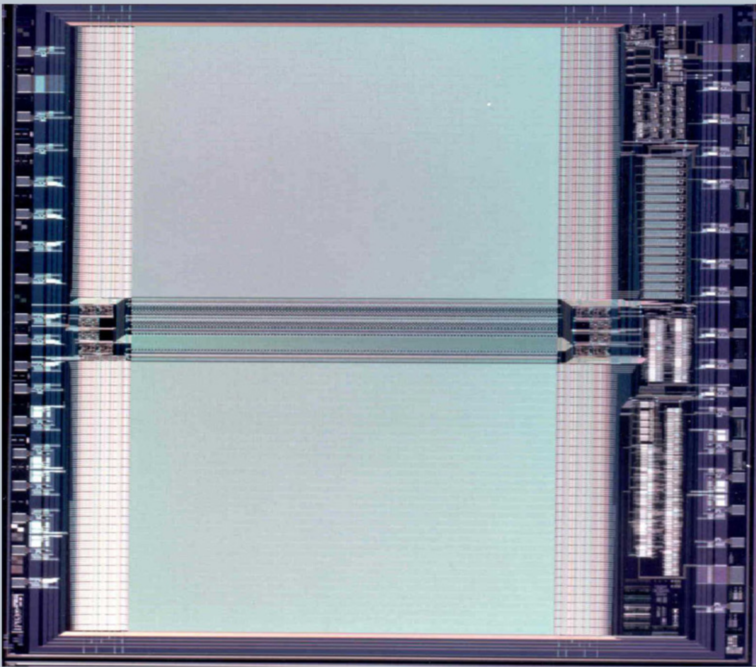

RADIATION HARDENED 128K X 8 CMOS EEPROM

Introduction

The W28C0108 radiation hardened nonvolatile 1Mbit (128K x 8) Electrically Erasable Programmable Read-Only Memory (EEPROM) is intended for use in space and harsh radiation environments where critical system data (Program Store, Start Up Read Only Memory, etc.) cannot be compromised during radiation exposure, or lost during power outages.

Features

- Rad Hard nonvolatile 1Mbit (128K x 8) EEPROM
  - >10,000 programming cycles
  - 100 year retention @ +125°C
  - <250 nsec read access time
  - 100 msec programming time
  - 3.3 Volt (Vdd) read operation
- Radiation Hardened
  - Total Dose up to 300 Krad (Si)
  - Transient Logic Upset > 1E8 rads(Si)/sec
  - Memory Data Loss > 1E12 rads(Si)/sec
  - SEU During READ LETth = 94 Mev-cm2 /mg
  - SEU in Address/Data Latches, LETth = 40 Mev-cm2/mg
  - Permanent SEU damage (During Write Only), Atomic Number > Kr
  - No SEL or data loss to to LET> 94 Mev-cm2 /mg
- No Latchup
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.
- JEDEC pin compatible in center 32 pins

Supports these commercial features:

- Self-Timed Programming
- Combined Erase/Write
- Auto Program Start
- Programming Voltage Internally Generated (Low Dose application only)
- Asynchronous Addressing
- 128 Word Page
- Data Polling
- All devices screened for memory cycling (500 cycles) and memory retention (>10 years)

Proven Technology

The W28C0108 is the next device in a family of successful Northrop Grumman radiation hardened EEPROM devices that already includes 64K and 256K EEPROM devices. The radiation hardened robustness of the design (performed by Sandia National Laboratories) and fabrication process is flight proven with more than 10,000 radiation hardened EEPROM devices previously delivered to production systems. This product line offers the only solid-state reprogrammable nonvolatile memory available today that is inherently radiation hardened. No special shielding, specialized packages, redundant devices, or special power down is required to operate these devices in severe radiation environments.

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Pinout (Top View)

36 PIN FLAT PACK

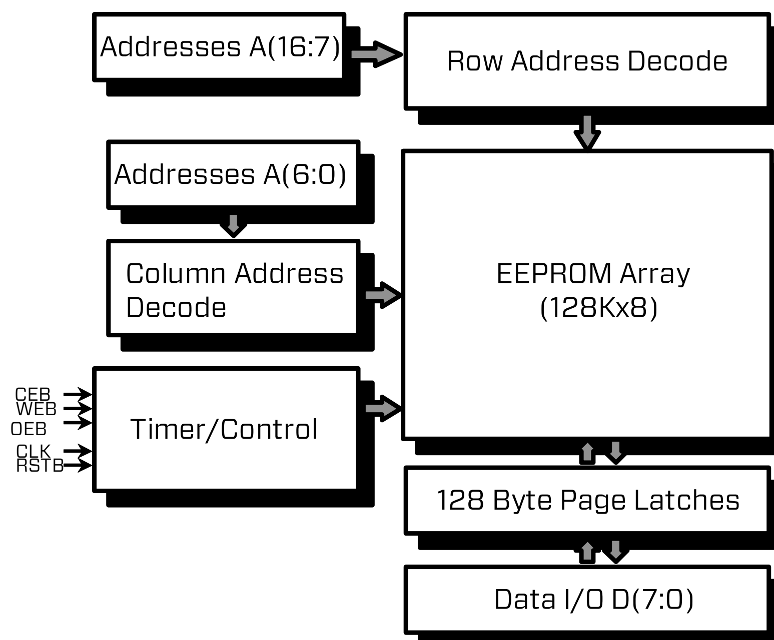
Signal	Pin	Pin	Signal
INHB	1	36	CPE
CCCP	2	35	VDD
A16	3	34	A14
A15	4	33	NC
A12	5	32	WRB_X
A7	6	31	A13
A6	7	30	A8
A5	8	29	A9
A4	9	28	A11
A3	10	27	OEB
A2	11	26	A10
A1	12	25	CEB
A0	13	24	D7
D0	14	23	D6
D1	15	22	D5
D2	16	21	D4
VSS	17	20	D3
CLK	18	19	VW

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
TSTG	Storage Temperature	-65 to +150*	°C
TA	Operating Temperature	-55 to +125	°C
VDDR	Power Supply During Read	6	V
VW	External Write Voltage with Respect to VDD	-8.5	V
VTERM	Terminal Voltage with Respect to Ground	6	V
TL	Lead Temperature (Soldering 10 Sec)	300	°C

* See data retention discussion on page 4.

1Mbit EEPROM Block Diagram



Caution: This device is sensitive to electrostatic discharge. Users should follow proper I.C. handling procedures.

Recommended Operating Conditions

Symbol	Parameter	Value	Units
Vdd	Positive Supply Voltage	3.3 +/- 0.17	Volts
Vss	Negative Supply Voltage	0 +/- 250mV	Volts
VW	Write Voltage	-4.2 +/- 0.21	Volts
T	Programming Time (CLK frequency 1.5MHz)	100	msec

DC Operating Characteristics

T_A = -55° to + 125°C, VDD = 3.3V ± 5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
IDDS	Static I Read		10	mA	Read Mode, DC
IDDR (DIDD)	Active I Read		20	mA	Read Mode, 2 MHz
IDDW (IDE 3-6)	Active I Write		2	mA	Write Mode
IW1	Inactive I Write		25	uA	Standby or Read (Note 1)
IDDSB (IDE 1-2)	Standby I		1.5	mA	
IIH	Input I High		1	uA	
IIL	Input I Low	-1		uA	
IOH	Output I High		3	mA	VDD = 3.3V (Note 2)
IOL	Output I Low	-3		mA	VDD = 3.3V (Note 2)
VIL	Input V Low	0	0.66	V	VDD = 3.3V (Note 2)
VIH	Input V High	2.64	VDD	V	VDD = 3.3V (Note 2)
VOH	Output V High	2.64		V	VDD = 3.3 VW = -4.2 VIH = 2.5 VIL = 0.95 IOL = -3mA (Note 2)
VOL	Output V Low		0.66	V	VDD = 3.3 VW = -4.2 VIH = 2.5 VIL = 0.95 IOH = -3mA (Note 2)
IOZL	Tristate Leakage Low	-10		uA	
IOZH	Tristate Leakage High		10	uA	

Note 1: Tested but not recorded

Note 2: Verified by functional testing

Pin Descriptions

Addresses (A0-A16) - The address inputs select which byte will be accessed during a read or write operation. Addresses A0-A6 are the column or byte addresses and A7-A16 are the row or page addresses.

Data (D0-D7) - Data is written to or read from the part using these pins.

Chip Enable (CEB) - This input must be LOW during read and write operations. After a programming operation has been initiated, the part may be de-selected. When the part is de-selected, the outputs are tri-stated.

Output Enable (OEB) - This input controls the output buffers. When HIGH the outputs are tri-stated and when LOW the outputs are driven to the correct CMOS levels.

Write Enable (WRB) - This input controls the writing of data. The address is latched on the falling edge and the data is latched on the rising edge.

Oscillator input (CLK) - The oscillator input is used to time the programming functions and the nominal circuit design is for a 2MHz clock. The programming cycle requires 20,000 clock cycles (Twc = 10ms with a 2MHz clock). The programming cycle starts automatically after the 500 clock cycle Tblc wait time completes without an additional byte being written (Tblc = 250us with a 2MHz clock). The clock frequency can be in the range of 100kHz to 2MHz.

Inhibit input (INHB) - The inhibit input is active LOW and is used to prevent programming during power transitions or during high transient radiation environments. Commercial parts use internal circuitry to perform this function, but a more reliable alternative is to use an external signal that is active LOW. For ROM applications this input will be tied LOW.

VW input (VW) - The chip generates –4.2 Volts internally for low radiation applications. For high

transient and high total dose radiation environments, an external supply may be required. It can be supplied through this pin. IF THE INTERNAL VOLTAGE GENERATOR IS USED, THIS PIN MUST NOT BE CONNECTED. The internal charge pump is activated when the part is being programmed and the CPE is active.

Charge Pump Enable input (CPE) - This pin is used to control the charge pump. It is active HIGH. If the pin is HIGH and the part is programming, the charge pump will pump to 7.5V below VDD (–4.2V with VDD at +3.3V). There is a pull-down transistor on this pin, so the pin can be left floating if the charge pump is not used.

Chip Clear/Chip Program input (CCCP) - This pin is active HIGH. In normal applications the pin should always be held LOW. The pin is used during testing to cycle the entire memory. When the pin is HIGH the 128 bytes will be programmed into all of the pages, instead of just the addressed page.

Device Operation

Read

The part is placed in the read mode by forcing CEB LOW and WRB HIGH. The outputs are activated by bringing OEB LOW. The outputs will be in the high resistance state when either CEB or OEB are HIGH. After the first memory location is read, additional locations can be read by simply changing the address inputs while holding CEB and OEB LOW.

Write

Writing data into the memory is a two step process: loading 128 bytes into the data-in latches and then programming the latched data into a page of the memory. The page address is latched on chip when the first of the 128 bytes is written. A write is initiated when CEB and WRB are taken LOW. The last of the two signals to go LOW starts the write and the first to return HIGH terminates the write. The programming time for the SA3996 is controlled by an internal counter and the externally supplied clock input. After the last byte is written, the internal timer waits 500 clock cycles before starting the programming. The programming will automatically terminate 20,000 clock cycles after the programming starts (a total of 20,500 cycles after the last byte was written).

Ones Complement polling

The ones complement polling mode can be used to verify the completion of programming. If a read is performed on any address while the part is still being programmed (between 500 and 20,500 clock cycles after the last byte was written), the ones complement of the last byte written will be presented at the outputs. After programming has completed, a read of the last address written will result in the correct data being presented at the outputs. To monitor for completion of programming, the user can read the last address written until the correct data is read.

Data Retention

The W28C0108 EEPROM is based on SONOS nonvolatile memory technology. SONOS is an acronym for Silicon-Oxide-Nitride-Oxide-Silicon. The memory device is a polysilicon gate N-channel MOS transistor with a specially processed gate dielectric consisting of a tunnel oxide, a silicon nitride layer, and a capping oxide. SONOS technology is used in preference to conventional floating gate technology because of its superior reliability and radiation hardness. The SONOS memory effect relies on charge storage within the silicon nitride film, with the silicon dioxide above and below it acting as energy barriers to the loss of charge. The charge is injected by quantum mechanical tunnelling through the tunnel oxide. SONOS transistors are programmed with gate biases of -7.5 V for 75 msec during Erase and +7.5 V for 25 msec during Program. Transistor level testing indicates negligible change in memory retention (charge loss decay rates) after over 300,000 Program / Erase cycles. The 1M EEPROM device is conservatively specified for 10,000 cycles to avoid any possibility of retention failures associated with the combination of total dose radiation and endurance cycling.

All 1M EEPROM product receives a rigorous wafer level memory retention screen. Based on a measured retention activation energy of 1.68 eV for this device, Arrhenius equation calculations predict that the 1M EEPROM will have a memory retention failure rate of < 0.1% at 250 years at +125 C (95% level of confidence). For operation beyond 100 krad(Si), data should be written after every 100 krad(Si) of accumulated total ionizing dose. In addition to the memory devices themselves, a key feature of this device is the radiation hardened peripheral circuitry. This circuitry remains virtually unaffected by radiation effects within the limits specified over the full range of device operation.

For proper retention and reliability, the memory devices require careful control of the clear/write conditions. This applies particularly to the control of the clear/write voltage. The clear/write time (pulsewidth) is also important. Consequently, both a Clock pin and a Vwrite pin are provided. With a nominal 0.15 MHz clock and Vw = -4.2V±5%, this device emulates commercial EEPROMs. Under these conditions, data retention is guaranteed for a minimum of 10 years at +125 C. The external clock is required for write mode only, read mode is asynchronous and no clock is required.

Programming Example

The memory is divided into 1024 pages with 128 bytes in each page. The bytes within a page can be written in any order and the pages can be programmed in any order. The following example writes the 8k bytes in order from address 0000h to address 1FFFh.

Hold INHB LOW

Force VDD to +3.3V

Force VW to –4.2V

Switch INHB HIGH

Write byte 0,page 0 {A(6:0)=0000000,A(16:7)=0000000000,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 1,page 0 {A(6:0)=0000001,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 2,page 0 {A(6:0)=0000010,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 126,page 0 {A(6:0)=1111110,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 127,page 0 {A(6:0)=1111111,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Wait 10.25ms or data poll after 250us

Write byte 0,page 1 {A(6:0)=0000000,A(16:7)=0000000001,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 1,page 1 {A(6:0)=0000001,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 2,page 1 {A(6:0)=0000010,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 126,page 1 {A(6:0)=1111110,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 127,page 1 {A(6:0)=1111111,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Wait 10.25ms or data poll after 250us

:

: repeat for pages 2-1022

:

Write byte 0,page 1023 {A(6:0)=0000000,A(16:7)=1111111111,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 1,page 1023 {A(6:0)=0000001,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 2,page 1023 {A(6:0)=0000010,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 126,page 1023 {A(6:0)=1111110,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Write byte 127,page 1023 {A(6:0)=1111111,A(16:7)=xxxxxxxxxx,CEB=0,WEB=0,OEB=1,D=data-in}

Wait 10.25ms or data poll after 250us

Read entire memory to verify contents

Switch INHB LOW

Force VW to 0V

Force VDD to 0V (along with any inputs not at 0V)

- END -

1Mbit EEPROM Pin Designation for 36 Pin Package

Package Pin	Package Function Name	Die Pad	Die Function Name	Function
NC	NC	43	VSS	*
NC	NC	44	VDD	*
1	INHB	1	INHB	I
2	CCCP	2	CCCP	I
3	A16	3	A16	I
4	A15	4	A15	I
5	A12	5	A12	I
6	A7	6	A7	I
7	A6	7	A6	I
8	A5	8	A5	I
9	A4	9	A4	I
10	A3	10	A3	I
11	A2	11	A2	I
12	A1	12	A1	I
13	A0	13	A0	I
14	D0	14	D0	I/O
15	D1	15	D1	I/O
16	D2	16	D2	I/O
17	VSS	17	VSS	*
18	CLK	18	CLK	I
NC	NC	19	VDD	*
NC	NC	20	CLK	I

Package Pin	Package Function Name	Die Pad	Die Function Name	Function
NC	NC	42	CPE	I
NC	NC	41	VSS	I
36	CPE	40	CPE	I
35	VDD	39	VDD	*
34	A14	38	WRB	I
33	NC	37	A14	I
32	WRB_X	36	WRB_X	I
31	A13	35	A13	I
30	A8	34	A8	I
29	A9	33	A9	I
28	A11	32	A11	I
27	OEB	31	OEB	I
26	A10	30	A10	I
25	CEB	29	CEB	I
24	D7	28	D7	I/O
23	D6	27	D6	I/O
22	D5	26	D5	I/O
21	D4	25	D4	I/O
20	D3	24	D3	I/O
NC	NC	23	VDD	*
19	VW	22	VW	*
NC	NC	21	VSS	*

Note 1: * Indicates a power supply pin

Operation Mode Truth Table

Mode	CEB	OEB	WRB	INHB	CCCP	A(16:0)	I/O
Read	Vil	Vil	Vih	X	X	Addr	Dout
Standby	Vih	X	X	X	X	XXX	Hi Z
Write	Vil	Vih	Vil	Vih	Vil	Addr	Din
Write Inhibit	X	X	X	Vil	X	XXX	Hi Z/Dout
Cycling	Vil	Vih	Vil	Vih	Vih	Addr	Din

AC Operating Characteristics (Write Operations)

Guaranteed by design but not tested

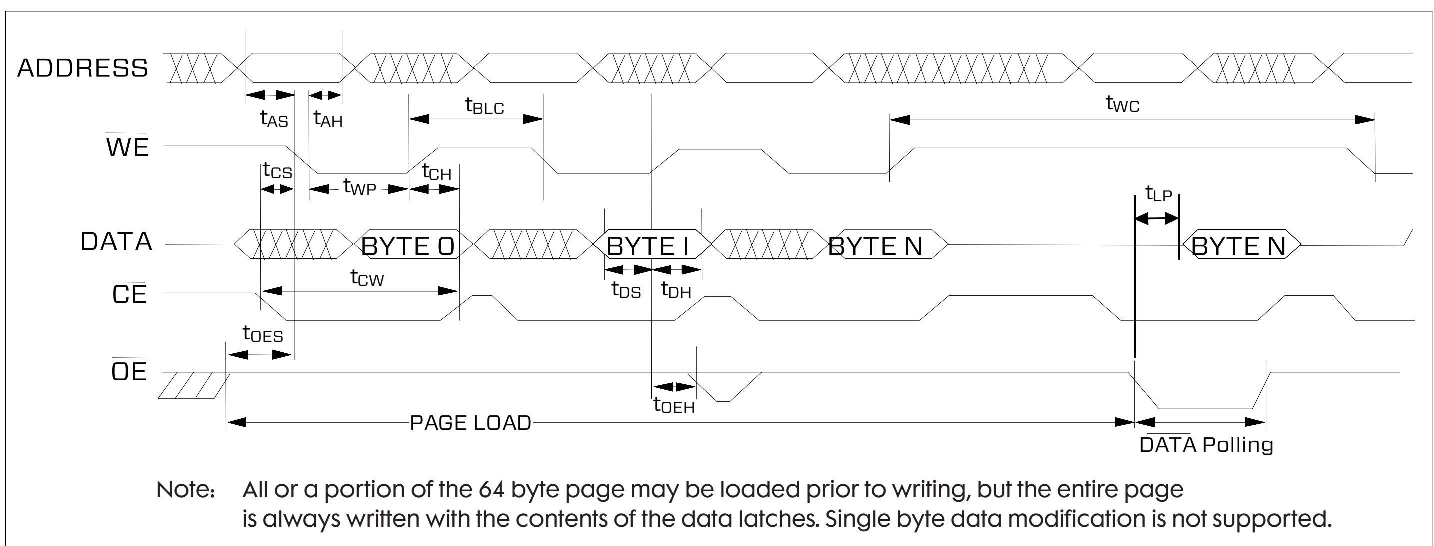
Recommended Operating Conditions: T_A = -55 to + 125°C, VDD = 3.3V ± 5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
^tC	Clock Frequency	0.15	0.2	MHz	Write Mode (Note 1) 0.15 MHz recommended for greater than 10 year memory retention
^tWC	Write Cycle Time		100	ms	Scales with Clock Frequency
^tAS	Address Setup time	0		ns	
^tAH	Address Hold Time	150		ns	
^tCS	Write Setup Time	0		ns	
^tCH	Write Hold Time	0		ns	
^tCW	CEB Pulse Width	150		ns	
^tOES	OEB High Setup Time	10		ns	
^tOEH	OEB High Hold Time	10		ns	
^tWP	WEB Pulse Width	150		ns	
^tDS	Data Setup Time	25		ns	
^tDH	Data Hold Time	60		ns	
^tBLC	Byte Load Cycle	499		CLK Cycles	(Note 1)
^tLP	Last Byte Loaded to Data Polling Output	499		CLK Cycles	(Note 1)

Note 1: Verified by functional testing.

Note 2: Correct by design, not functionally tested.

Write Cycle



Note: All or a portion of the 64 byte page may be loaded prior to writing, but the entire page is always written with the contents of the data latches. Single byte data modification is not supported.

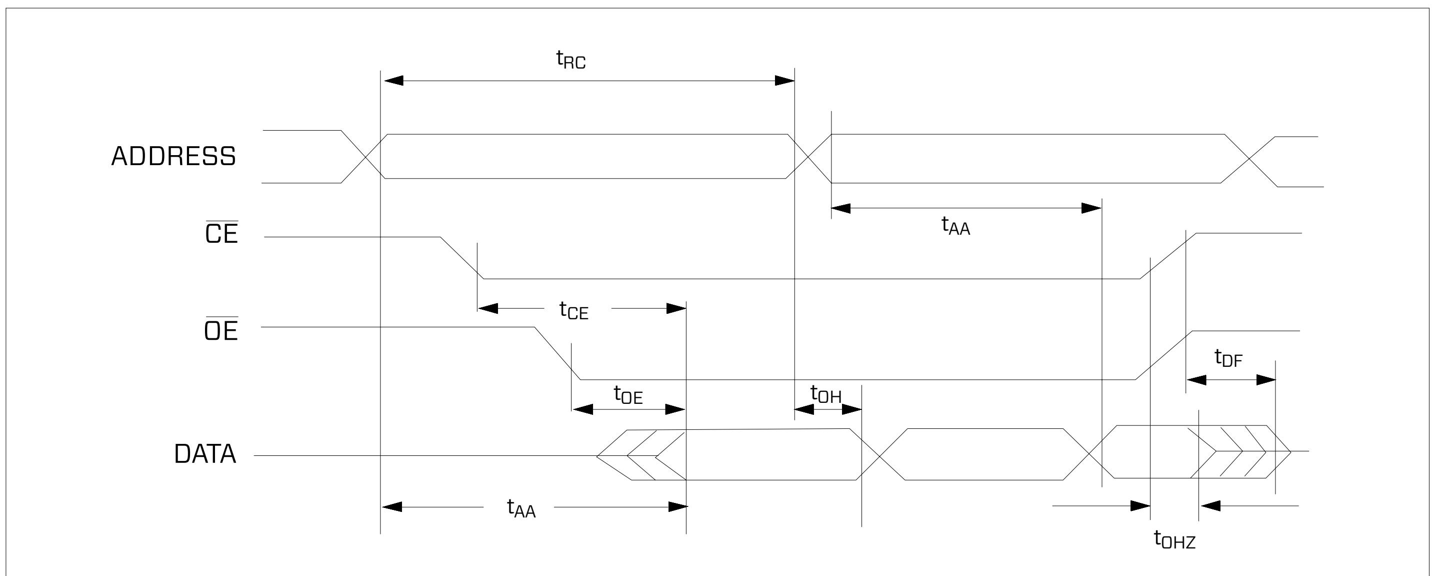
AC Operating Characteristics (Read Operations)

Recommended Operating Conditions: T_A = -55 to +125°C, VDD =3.3V ± 5%, unless otherwise specified

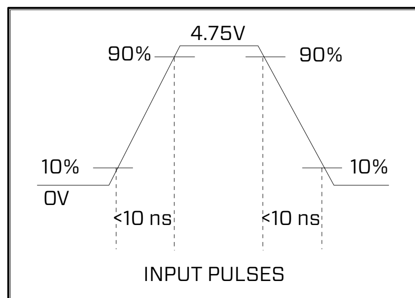
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
t_{RC}	Read Cycle Time	250		ns	
t_{CE}	CEB Access time		250	ns	OEB = VIL
t_{AA}	Address Access Time		250	ns	CEB = OE = VIL
t_{OE}	OE Access Time		90	ns	CEB = VIL
t_{DF}	OE or CE High to Output Hi Z	0	130	ns	CE = OE = VIL Load current = 3mA
t_{OH}	Output Hold from Address Change	0		ns	CE = OE = VIL (Note 1)
t_{OHZ}	DEB High to High Z Output	25		ns	Load current = 3mA

Note 1: Guaranteed but not tested.

Read Cycle



AC Test Loads and Input Waveforms



Capacitance T_A = 25°C f = 1 MHz

Symbol	Parameter	MAX	Conditions
C_{IN}	Input Capacitance	5 pF	Vin = 0
C_{OUT}	External Load Capacitance	70 pF	AC Operations

1Mbit Dynamic Burn-In Circuit

Pin	Resistor	Connection
A(16:0)	3.0K	Vector
D(7:0)	2.2K	VDD/2
CEB	3.0K	VSS
WRB	3.0K	VDD
OEB	3.0K	VSS
WRB_X	3.0K	VDD
CLK	3.0K	VSS
CPE	3.0K	VSS
CCCP	3.0K	VSS
INHB	3.0K	VSS
VW	-	VSS
VSS	-	0 V
VDD	-	3.6V

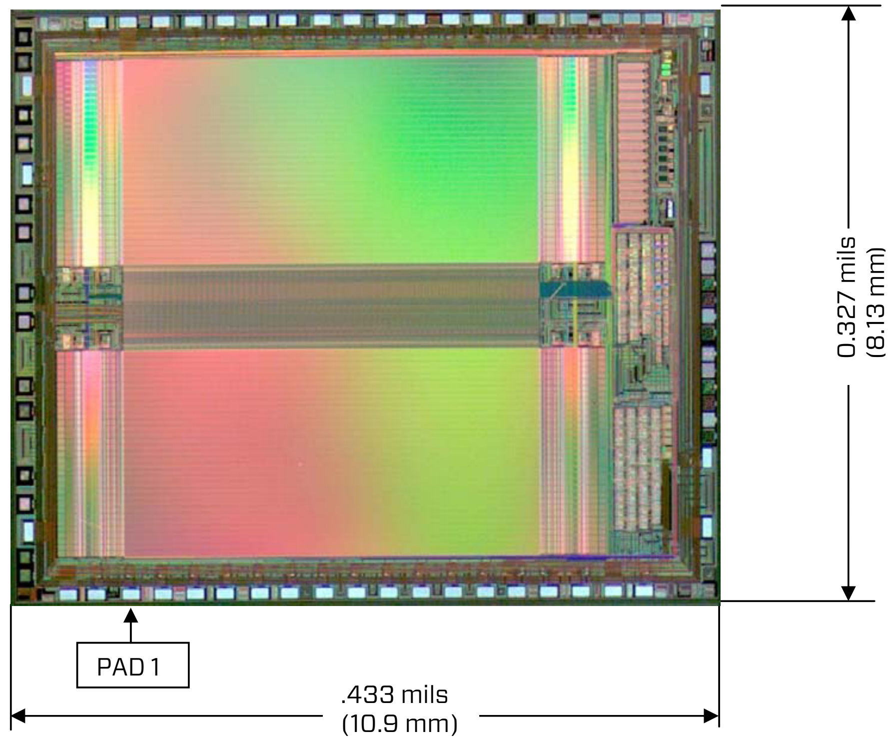
1Mbit Static Burn-In Circuit

Pin	Resistor	Connection
A(16,14,12,10,8,6,4,2,0)	3.0K	VSS
A(15,13,11,9,7,5,3,1)	3.0K	VDD
D(7:0)	2.2K	VDD/2
CEB	3.0K	VSS
WRB	3.0K	VDD
OEB	3.0K	VSS
WRB_X	3.0K	VDD
CLK	3.0K	VSS
CPE	3.0K	VSS
CCCP	3.0K	VSS
INHB	3.0K	VSS
VW	-	VSS
VSS	-	0 V
VDD	-	3.6V

1Mbit Radiation Bias Circuit

Pin	Resistor	Connection
A(16,14,12,10,8,6,4,2,0)	3.0K	VSS
A(15,13,11,9,7,5,3,1)	3.0K	VDD
D(7:0)	2.2K	VDD/2
CEB	3.0K	VSS
WRB	3.0K	VDD
OEB	3.0K	VSS
WRB_X	3.0K	VDD
CLK	3.0K	VSS
CPE	3.0K	VSS
CCCP	3.0K	VSS
INHB	3.0K	VSS
VW	-	VSS
VSS	-	0 V
VDD	-	3.6V

W28C0108 Die Information



Structural Information

Die Dimensions.................... 430 x 327 x 23 mils

Metallization (2 levels)
Type.....................................TiN/Al-Cu / TiN
(N/ tungsten plugs)
Thickness.............................9.8 kÅ ± 1 kÅ

Glassivation
Type.....................................SiO_2 / SI_3N_4 / SiO_2
Thickness.............................12k Å ± 1 kÅ
Process CMS8RH

Die Attach
Material ....Gold Eutectic
Temperature ....400°C
Lead Temperature ......<275°C
(10 sec soldering)

36 Pin Flatpack

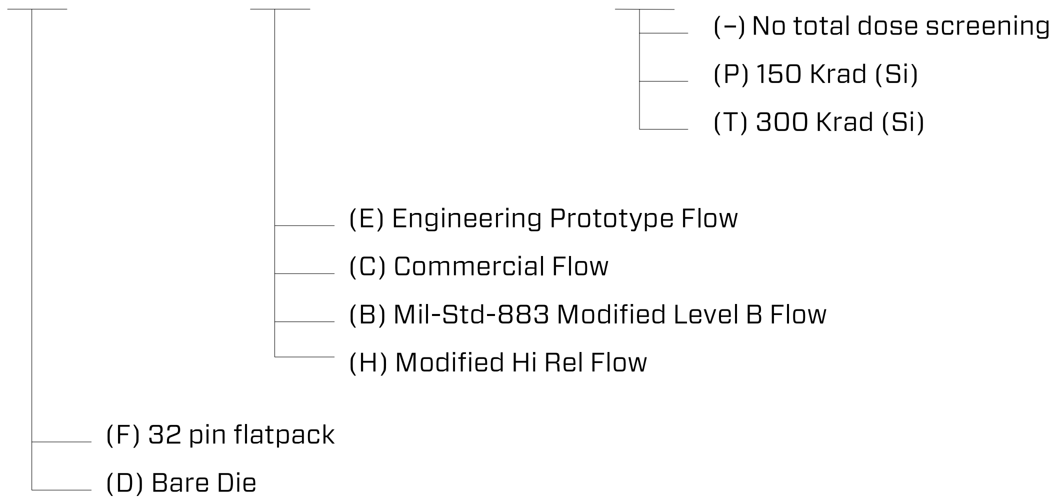
View A

View A

Ordering Information

To order the W28C0108 radiation hardened EEPROM, use the following part numbers.

W28C0108



Distribution is Unlimited; #21-0465; Dated 03/17/21
Specifications and features subject to change without notice.
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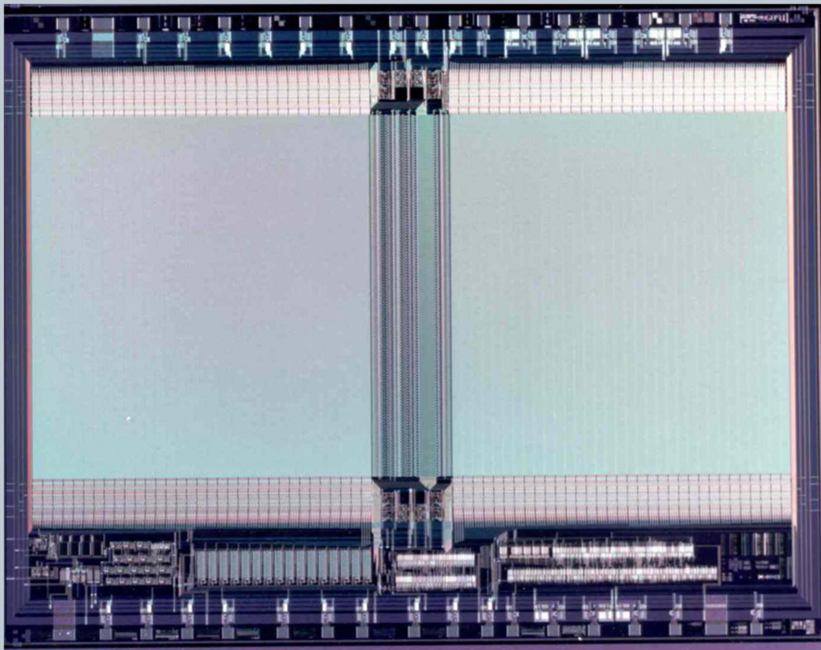
CS-16550-006 BWI | 2021

For more information, please contact:
Northrop Grumman Corporation
Mission Systems
Email: ATLFoundry@ngc.com



RADIATION HARDENED 32K X 8 CMOS EEPROM

Introduction

The W28C256 is a 32K x 8 radiation hardened EEPROM designed by Sandia National Laboratories, Albuquerque, NM, and manufactured by the Northrop Grumman Advanced Technology Center, Baltimore, MD, using nonvolatile memory technology transferred from Sandia. It is built using a mature dual well CMOS process using N on N+ epitaxial silicon and a two layer interconnect system.

Features

- 1.25 Micrometer Radiation Hardened CMOS on Epi
  - Total Dose up to 300 Krad (Si)
  - Transient Logic Upset >5E7 Rad(Si)/sec
  - Memory Data Loss >1E12 Rad(Si)/sec
- Single Event Upsets
  - SEU During READ LETth = 60 MeV/mg/cm^2
  - SEU in Address/Data Latches, LETth = 35 MeV/mg/cm^2
  - Permanent SEU damage (During Write Only), Atomic Number W$\geq$ Kr
- No Latchup
- Compatible with commercial EEPROMs
- JEDEC pin compatible in center 28 pins
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.

Supports these commercial features:

- Self-Timed Programming
- Combined Erase/Write
- Auto Program Start
- +5V only read operation
- Asynchronous Addressing
- 64 Word Page
- Data Polling

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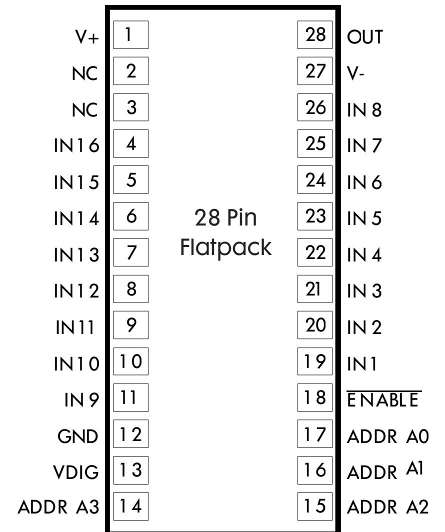
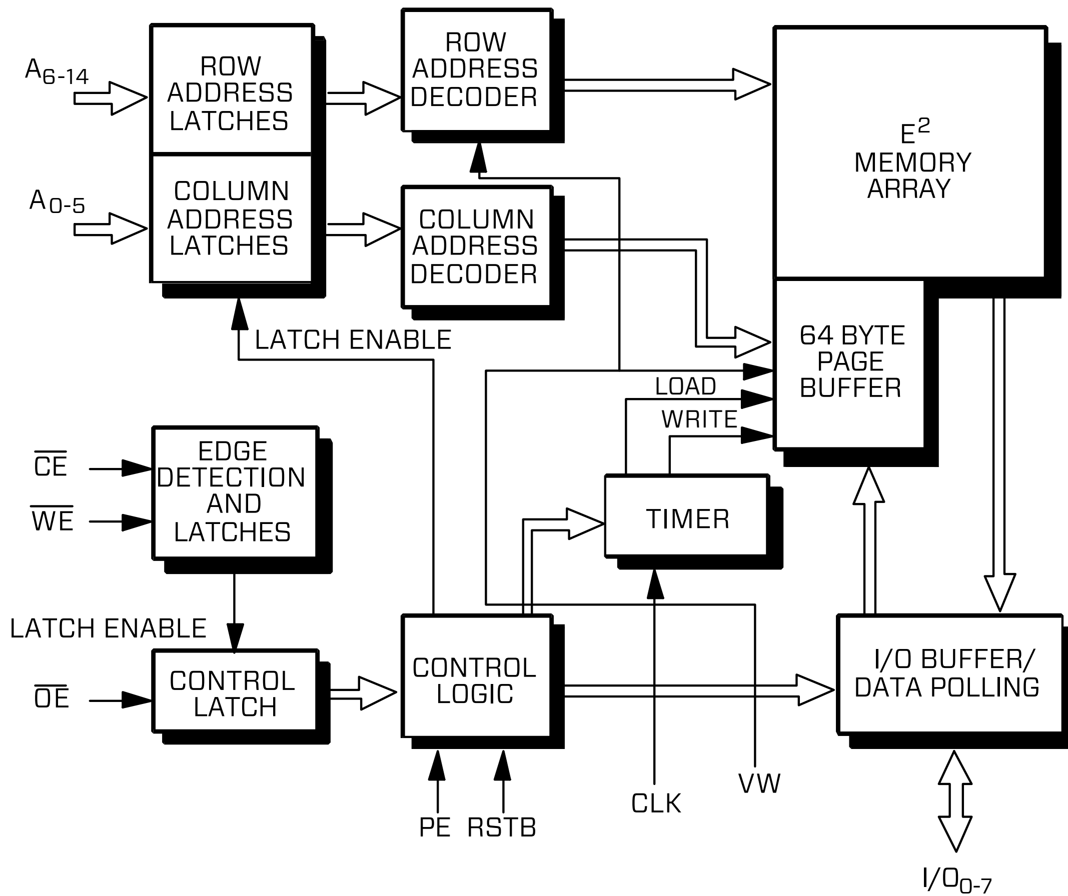
Absolute Maximum Ratings

Symbol	Parameter	Value	Units
TSTG	Storage Temperature	-65 to +150*	°C
TA	Operating Temperature	-55 to +125	°C
VDDR	Power Supply During Read	6	V
VW	External Write Voltage with Respect to VDD	-10.5	V
VTERM	Terminal Voltage with Respect to Ground	6.5	V
TL	Lead Temperature (Soldering 10 sec)	300	°C

* See data retention discussion on page 4.



Pinout
(Top View)



DC Operating Characteristics: W28C256

T_A = -55° to +125°C, VDD = 5V ±5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
IDDS	Static I Read		10	mA	Read Mode, DC
IDDR	Active I Read		17	mA	Read Mode, 2 MHz
IDDW	Active I Write		2	mA	Write Mode
IW1	Inactive I Write	-25		uA	Standby or Read (Note 1)
IDDSB	Standby I		1.5	mA	
IIH	Input I High		1	uA	
IIL	Input I Low		1	uA	
IOH	Output I High		3	mA	VOH = 4.25V
IOL	Output I Low	-3		mA	VOL = 0.5V
VIL	Input V Low	-0.5	0.95	V	
VIH	Input V High	3.8	VDD +0.5	V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOL = -3mA (Note 2)
VOH	Output V High	4.25		V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOH = -3mA (Note 2)
VOL	Output V Low		0.5	V	
IOZL	Tristate Leakage Low	-10		uA	
IOZH	Tristate Leakage High		10	uA	

Note 1: Tested but not recorded

Note 2: Verified by functional testing

Mode Selection

Mode	CEB	OEB	WEB	PE	A(12:0)	I/O
Read	VIL	VIL	VIH	VIL	ADDR	DOUT
Standby	VIH	X	X	VIL	XXX	HI Z
Write	VIL	VIH	VIL	VIL	ADDR	DIN
Write Inhibit	X X	X VIL	VIH X	VIL VIL	XXX XXX	HI Z/DOUT HI Z/DOUT

Pin Description Addresses (A0-A14)

The address inputs select which byte will be accessed during a read or write operation. A0-A5 are the column or byte addresses and A6-A14 are the row or page addresses.

Chip Enable (CEB)

This input must be LOW during read and write operations. After a programming operation has been initiated, the chip may be deselected. When the part is deselected, the outputs are tristated.

Output Enable (OEB)

This input controls the output buffers. When HIGH the outputs are tristated and when LOW the outputs are driven to the correct CMOS levels.

Data (D0-D7)

Data is written to or read from the part using these pins.

Write Enable (WEB)

This input controls the writing of data. When low, write is enabled.

Clock Input (CLK)

The clock input is used to time the programming functions. The nominal value for a 10 ms write cycle is 2 MHz. The clock is not required for read operations. The clock waveform has no critical timing with respect to other input or output signals.

Reset Input (RSTB)

The reset input is active LOW and is used to prevent programming during power transitions or during high transient radiation doses. This signal should be held low during power up and power down.

Write Voltage (VW)

This -5V±5% supply pin is used to provide the internal programming voltage. This pin may be tied to OV during read operations. During power up VDD must come up first, then Vw; and during power down Vw must go off first, then VDD.

Program Enable Input (PE)

This pin is used for testing and validation purposes to gain more control over internal chip operation. Normal operation requires this pin to be tied LOW.

Data Polling

The programming time for the W28C256 is controlled by an internal counter and the externally supplied clock input. The nominal timing is for a 10 ms programming time with a 2 MHz clock input. The Data Polling mode can be used to verify the completion of programming. If a read is performed on any address while the part is still being programmed, the ones complement of the last byte written will be presented at the outputs. After programming has completed, a read of the last address written will result in the correct data being presented at the outputs. To monitor for completion of programming the user can read the last address written until the correct data is read.

Data Retention

The W28C256 EEPROM is based on SONOS nonvolatile memory technology. SONOS is an acronym for Silicon-Oxide-Nitride-Oxide-Silicon. The memory device is a silicon gate N-channel MOS transistor with a specially processed gate dielectric consisting of a tunnelling oxide, a silicon nitride layer, and a capping oxide. SONOS technology is used in preference to conventional floating gate technology because of its superior reliability and radiation hardness. The SONOS memory effect relies on charge storage within the silicon nitride film, with the silicon dioxide above and below it acting as energy barriers to the loss of charge. The charge is injected by tunnelling through the tunnelling oxide.

The charge deposited in the SONOS dielectric does decay slowly with time, but when written under the specified conditions and stored within the specified limits, data is indeed permanent for most purposes. Data loss is accelerated by both temperature and radiation, and is also affected by the number of write cycles the device has seen previously.

Write cycles must, however, be accumulated in the tens of thousands before any effect on retention is seen. When written using a 2 MHz external clock, nonvolatile data storage is guaranteed through 100 K Rad (Si), without rewriting, at the specified temperature range. In satellite applications, this normally corresponds to many years of service.

For operation beyond 100 K Rad (Si), data should be written after every 100 K Rad of accumulated total dose. In addition to the memory devices themselves, a key feature of this device is the radiation hardened peripheral circuitry. This circuitry remains virtually unaffected by radiation effects within the limits specified over the full range of device operation.

For proper retention and reliability, the memory devices require careful control of the clear/write conditions. This applies particularly to the control of the clear/write voltage. The clear/write time (pulsewidth) is also important.

Consequently, both a Clock pin and a Vwrite pin are provided. With a nominal 2 MHz clock and Vw = -5V±5%, this device emulates commercial EEPROMs. Under these conditions, data retention is guaranteed for a minimum of 10 years. The external clock is required for write mode only, read mode is asynchronous and no clock is required.

Temperature	Retention (Years)	Cycles	Total Dose K Rad (Si)
-55 to 80°C	10	10,000	0 to 50
-55 to 80°C	10*	1,000	50 to 100

Rewriting after 100 K Rads results in another 10 years of retention up to a max total dose specified

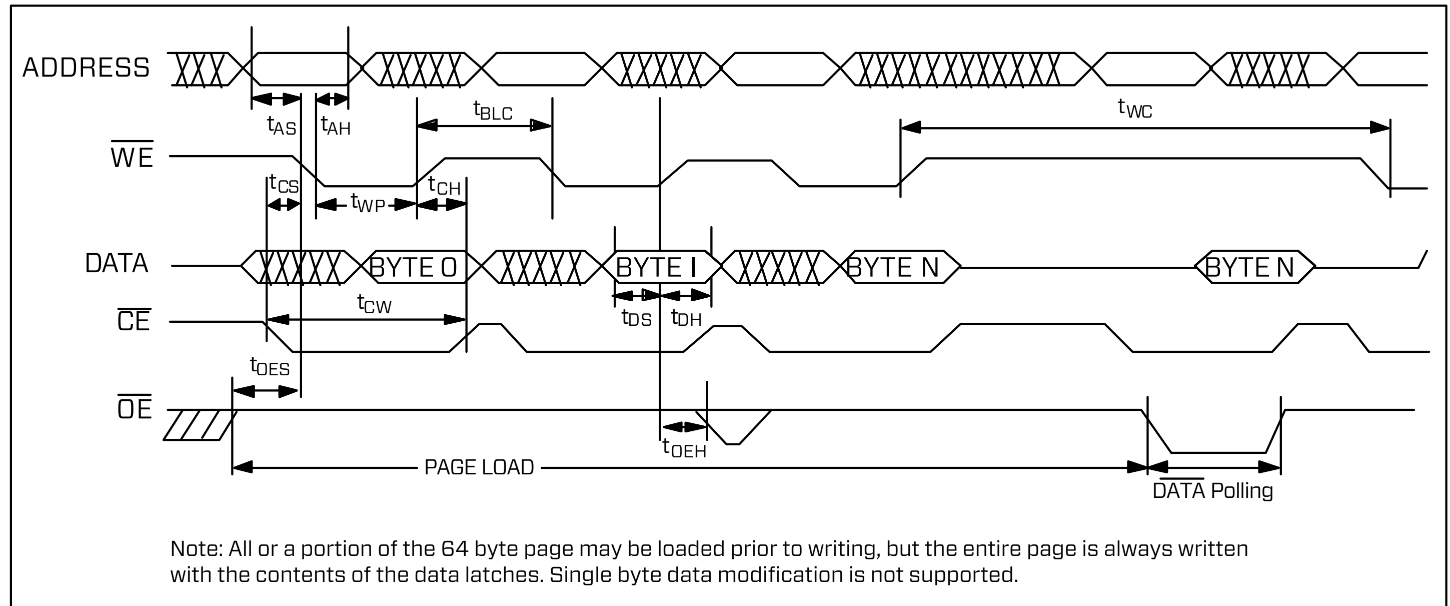
AC Operating Characteristics (Write Operations)

T_A = -55° to +125°C, VDD = 5V ±5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
^{t}C	Clock Frequency	1	2	MHz	Write Mode (Note 1)
^{t}WC	Write Cycle Time		10	ms	fc = 2 MHz (Note 1)
^{t}AS	Address Setup Time	0		ns	
^{t}AH	Address Hold Time	150		ns	
^{t}CS	Write Setup Time	0		ns	
^{t}CH	Write Hold Time	0		ns	
^{t}CW	CEB Pulse Width	150		ns	
^{t}OES	OEB High Setup Time	10		ns	
^{t}OEH	OEB High Hold Time	10		ns	
^{t}WP	WEB Pulse Width	150		ns	
^{t}DS	Data Setup Time	0		ns	
^{t}DH	Data Hold Time	60		ns	
^{t}BLC	Byte Load Cycle	0.2	250	^{x}S	fc = 2 MHz
^{t}LP	Last Byte Loaded to Data Polling Output	300		^{x}S	fc = 2 MHz

Note 1: Verified by functional testing.

Write Cycle



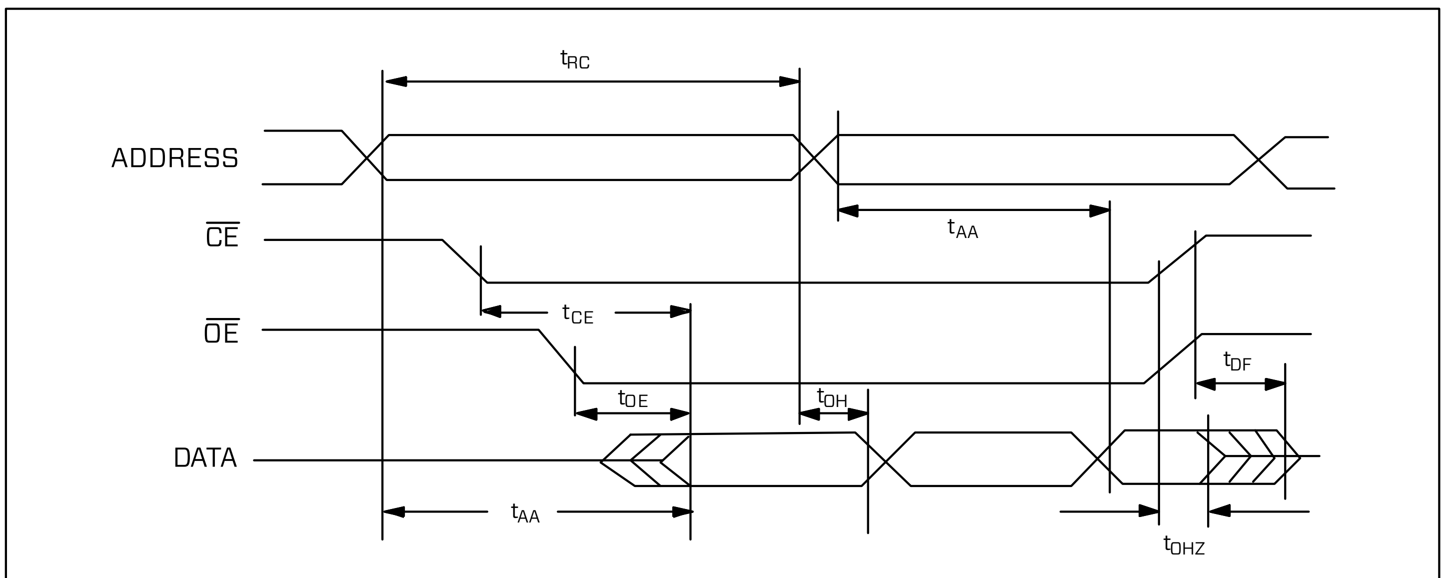
AC Operating Characteristics (Read Operations)

T_A = -55° to +125°C, VDD = 5V ±5%, unless otherwise specified

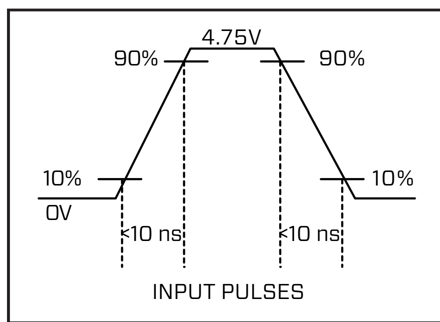
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
^tRC	Read Cycle Time	250		ns	
^tCE	CEB Access Time		250	ns	OEB = VIL
^tAA	Address Access Time		250	ns	CEB = OEB = VIL
^tOE	OEB Access Time		125	ns	CEB = VIL
^tDF	OEB or CEB High to Output High Z		130	ns	CEB OR OEB = VIL IO = ±3mA
^tOH	Output Hold from Address Change	0		ns	CEB = OEB = VIL (Note 1)
^tOHZ	OEB High to High Z Output	25		ns	IO = ±3mA

Note 1: Verified by functional testing.

Read Cycle

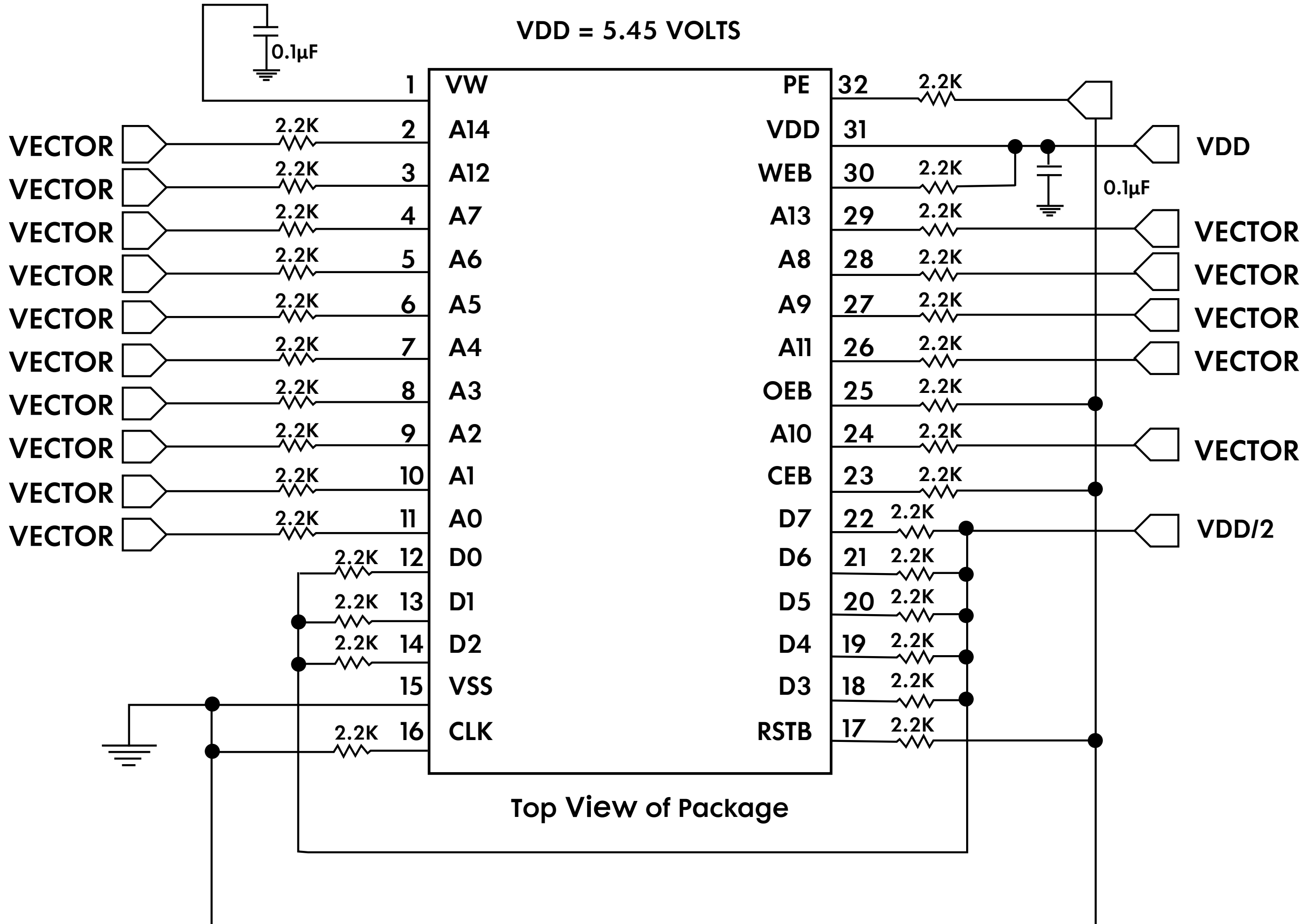


AC Test Loads and Input Waveforms

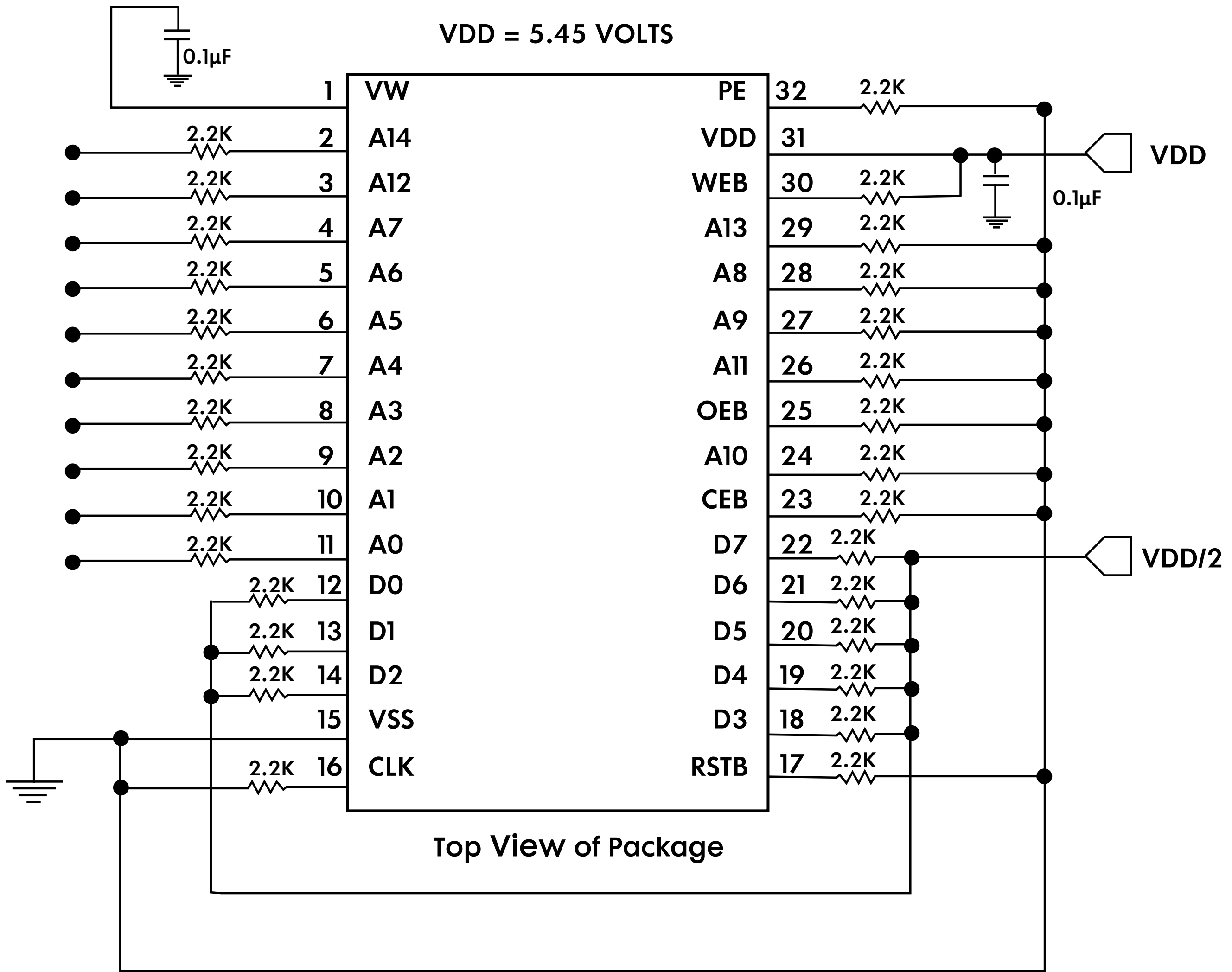


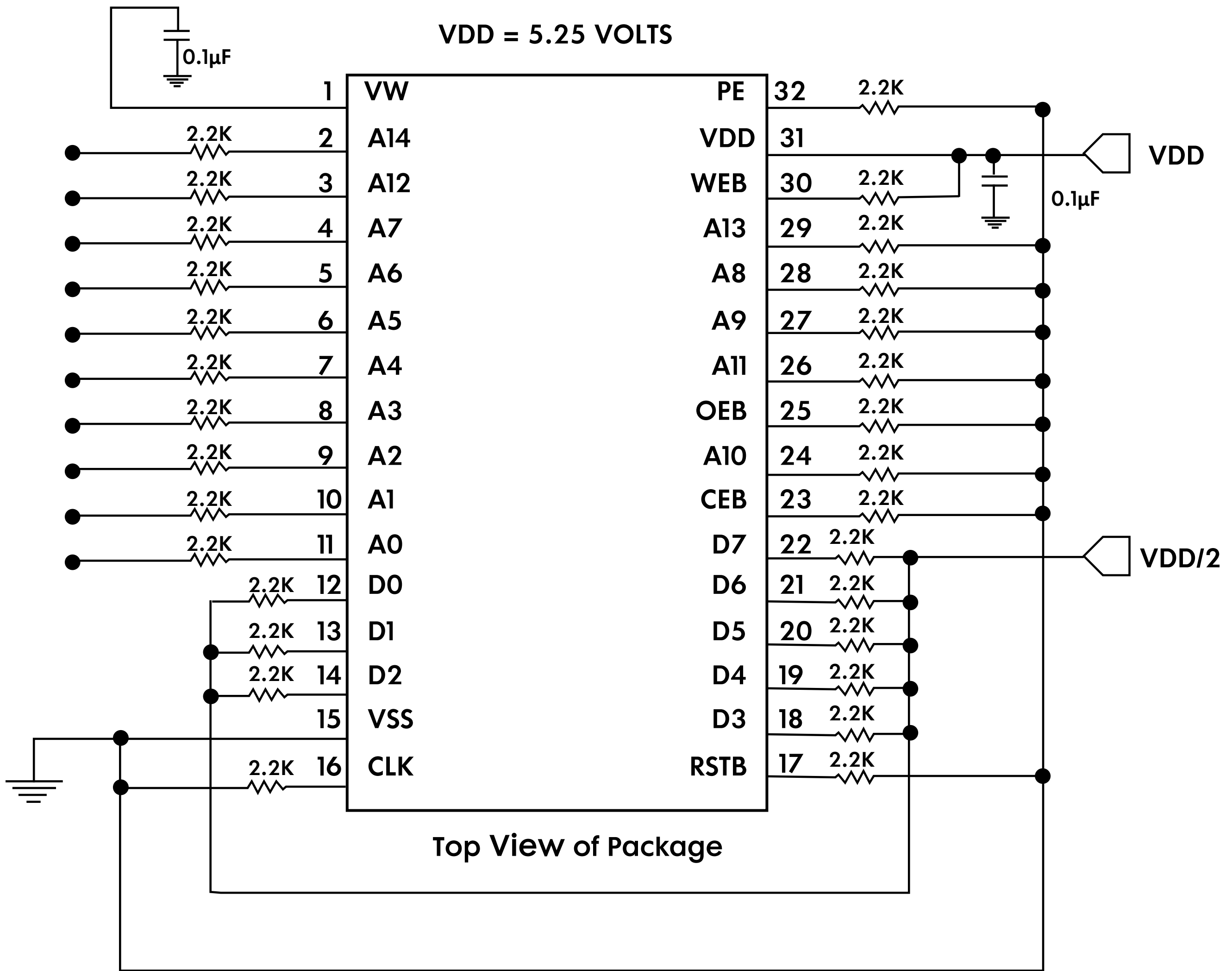
CAPACITANCE T_A = 25°C f = 1 MHz

Symbol	Parameter	MAX	Conditions
C_{IN}	Input Capacitance	5pF	Vin = 0
C_{OUT}	External Load Capacitance	70pF	AC Operations

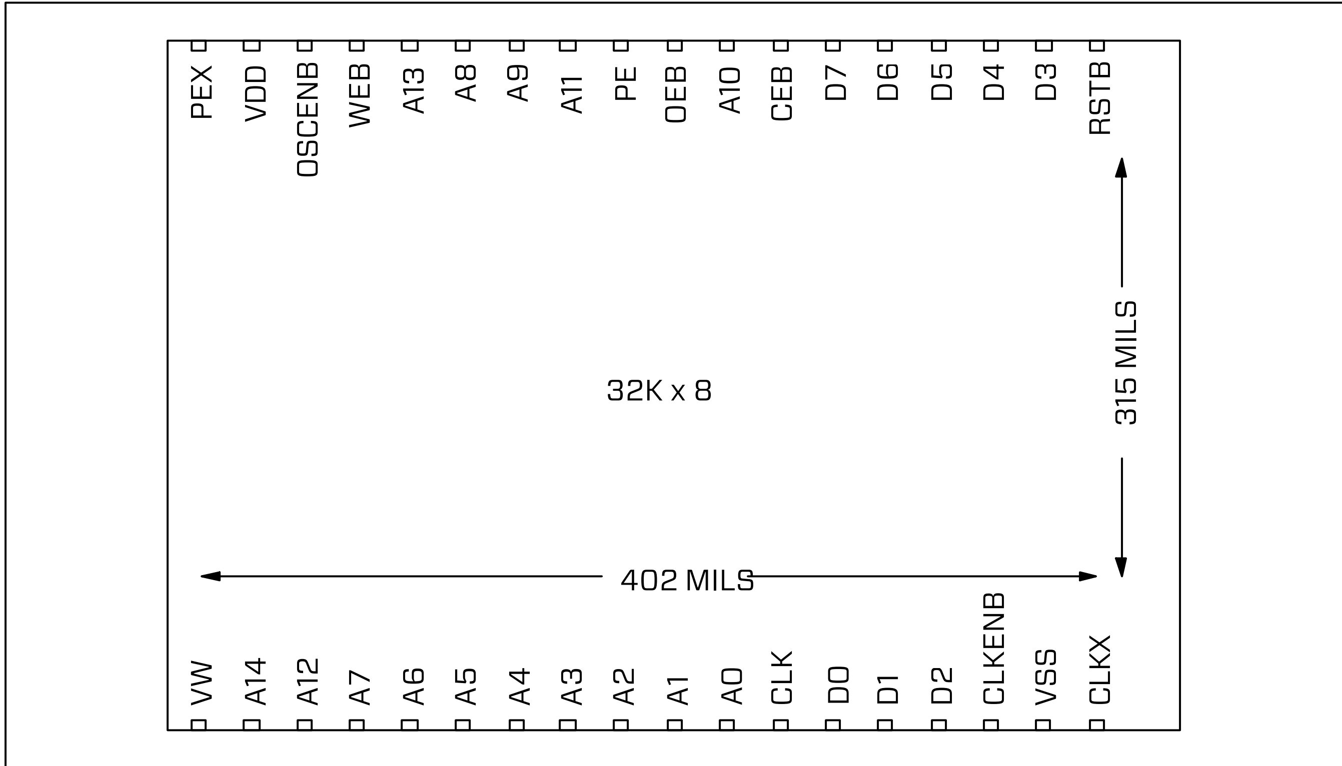


Dynamic Burn-in Circuit
VDD = 5.45 VOLTS
0.1µF
1 VW
2 A14
3 A12
4 A7
5 A6
6 A5
7 A4
8 A3
9 A2
10 A1
11 A0
12 D0
13 D1
14 D2
15 VSS
16 CLK
PE 32
VDD 31
WEB 30
A13 29
A8 28
A9 27
A11 26
OEB 25
A10 24
CEB 23
D7 22
D6 21
D5 20
D4 19
D3 18
RSTB 17
2.2K
VECTOR
VDD
VDD/2
0.1µF
Top View of Package
Notes:
1. VW = GND
2. RSTB = GND


Static Bias Circuit
VDD = 5.45 VOLTS
0.1µF
1 VW
2 A14
3 A12
4 A7
5 A6
6 A5
7 A4
8 A3
9 A2
10 A1
11 A0
12 D0
13 D1
14 D2
15 VSS
16 CLK
PE 32
VDD 31
WEB 30
A13 29
A8 28
A9 27
A11 26
OEB 25
A10 24
CEB 23
D7 22
D6 21
D5 20
D4 19
D3 18
RSTB 17
2.2K
VDD
0.1µF
VDD/2
Top View of Package
Notes:
1. VW = GND
2. RSTB = GND

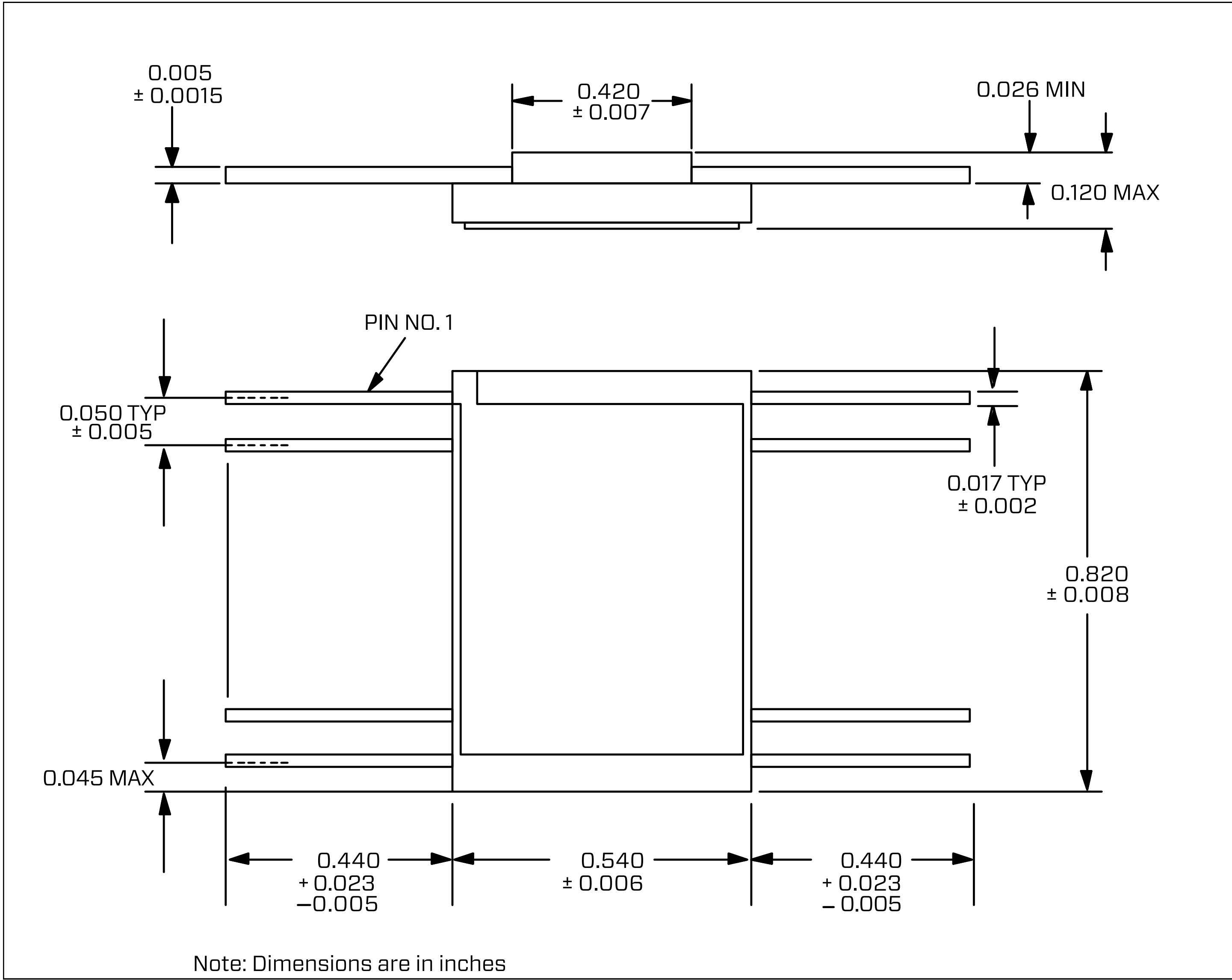

Radiation Bias Circuit
VDD = 5.25 VOLTS
0.1µF
1 VW
2 A14
3 A12
4 A7
5 A6
6 A5
7 A4
8 A3
9 A2
10 A1
11 A0
12 D0
13 D1
14 D2
15 VSS
16 CLK
PE 32
VDD 31
WEB 30
A13 29
A8 28
A9 27
A11 26
OEB 25
A10 24
CEB 23
D7 22
D6 21
D5 20
D4 19
D3 18
RSTB 17
2.2K
VDD
VDD/2
0.1µF
Top View of Package
Notes: 1. VW = GND

W28C256 Die Information



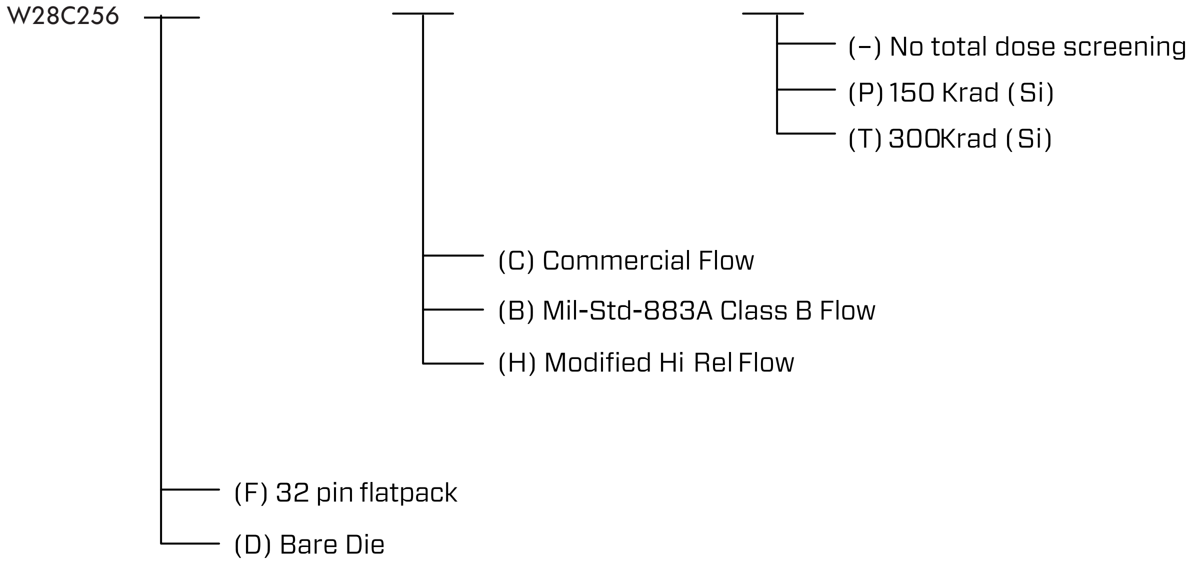
CLKENB : An internal oscillator enable pin, has internal pullup to keep disabled.
CLKX : A redundant CLKIN pin. CLKIN and CLKX are internally connected.
PEX : A redundant PE pin. PE and PEX are internally connected.
OSCENB : Similar to CPEB on 64K. This will enable the on board charge pump and eliminate the need for VW (-5V). There is an internal pull down to keep the charge pump disabled, OSCENB is active hi.

32 PinFlatpack



Ordering Information

To order the W28C256 radiation hardened EEPROM, use the following part numbers.



Distribution is Unlimited; #21-0465; Dated 03/17/21
Specifications and features subject to change without notice.
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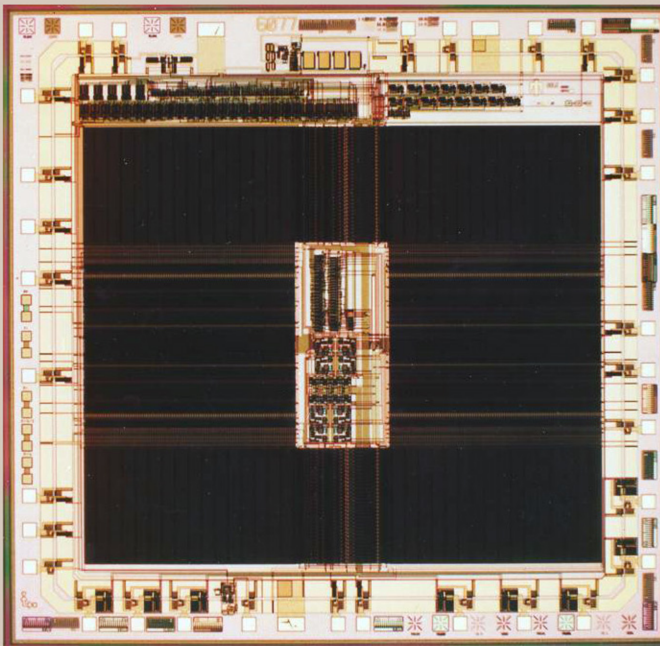
CS-16550-007 BWI | 2021

For more information, please contact:
Northrop Grumman Corporation
Mission Systems
Email: ATLFoundry@ngc.com



RADIATION HARDENED 8K X 8 CMOS EEPROM

Introduction

The W28C64 is a 8K x 8 radiation hardened EEPROM designed by Sandia National Laboratories, Albuquerque, NM, and manufactured by Northrop Grumman Advanced Technology Center, Baltimore, MD, using nonvolatile memory technology transferred from Sandia. It is built using a mature dual well CMOS process using N on N+ epitaxial silicon and a two layer interconnect system.

Features

- 1.25 Micrometer Radiation Hardened CMOS on Epi
  - Total Dose up to 300 Krad (Si)
  - Transient Logic Upset >5E7 Rad(Si)/sec
  - Memory Data Loss >1E12 Rad(Si)/sec
- Single Event Upsets
  - SEU During READ LETth = 60 MeV/mg/cm2
  - SEU in Address/Data Latches, LETth = 35 MeV/mg/cm2
  - Permanent SEU damage (During Write Only), Atomic Number ≥ Kr
- No Latchup
- Compatible with commercial EEPROMs
- JEDEC pin compatible in center 32 p LCC
- Full military operating temperature range, screened to specific test methods for commercial, Class B, or modified Hi Rel.

Supports these commercial features:

- Self-Timed Programming
- Combined Erase/Write
- Auto Program Start
- +5V only read operation
- Asynchronous Addressing
- 64 Word Page
- Data Polling

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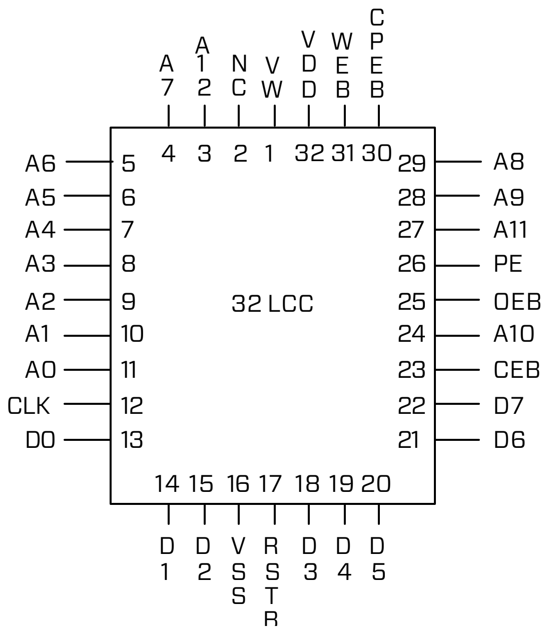
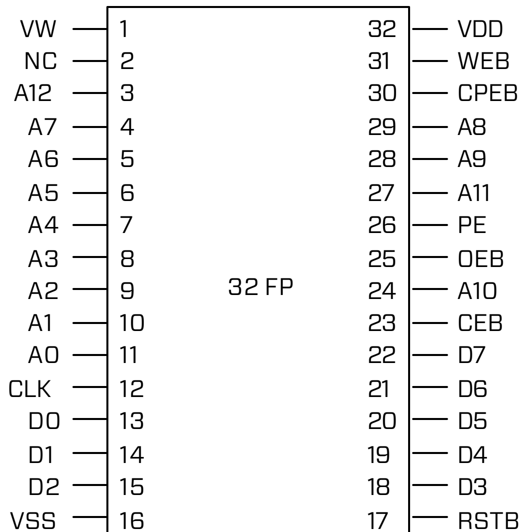
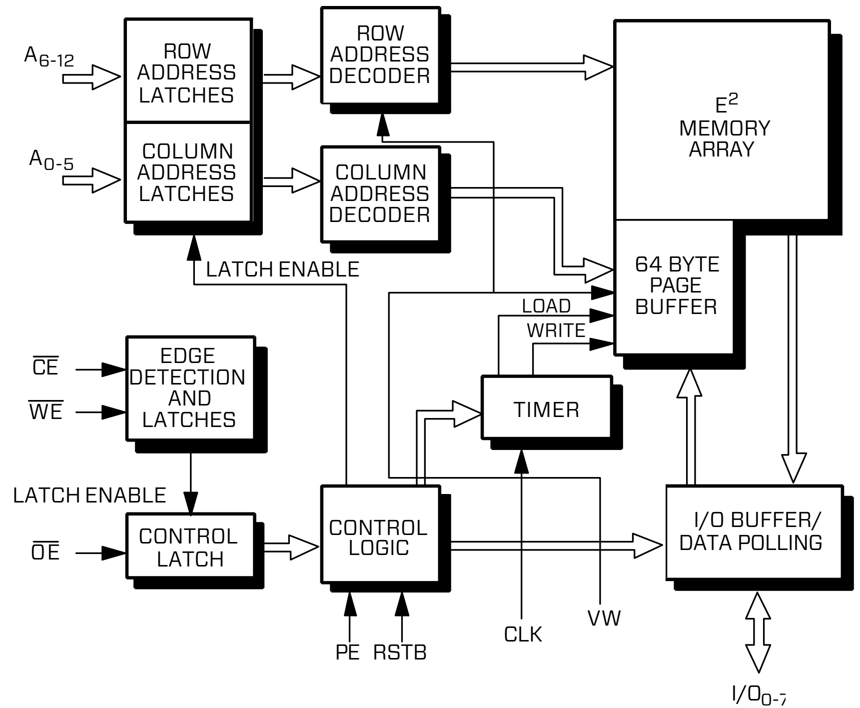






Absolute Maximum Ratings

Symbol	Parameter	Value	Units
TSTG	Storage Temperature	-65 to +150*	°C
TA	Operating Temperature	-55 to +125	°C
VDDR	Power Supply During Read	6	V
VW	External Write Voltage with Respect to VDD	-10.5	V
VTERM	Terminal Voltage with Respect to Ground	6.5	V
TL	Lead Temperature (Soldering 10 sec)	300	°C

* See data retention discussion on page 4.

DC Operating Characteristics

T_A = -55° to + 125°C, VDD = 5V ± 5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
IDDS	Static I Read		10	mA	Read Mode, DC
IDDR	Active I Read		17	mA	Read Mode, 2 MHz
IDDW	Active I Write		2	mA	Write Mode
IW1	Inactive I Write	-25		uA	Standby or Read (Note 1)
IDDSB	Standby I		1.5	mA	
IIH	Input I High		1	uA	
IIL	Input I Low		1	uA	
IOH	Output I High		3	mA	VOH = 4.25V
IOL	Output I Low	-3		mA	VOL = 0.5V
VIL	Input V Low	-0.5	0.95	V	
VIH	Input V High	3.8	VDD+0.5	V	
VOH	Output V High	4.25		V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOL = -3mA (Note 2)
VOL	Output V Low		0.5	V	VDD = 4.75 VW = -4.75 VIH = 3.8 VIL = 0.95 IOH = 3mA (Note 2)
IOZL	Tristate Leakage Low	-10		uA	
IOZH	Tristate Leakage High		10	uA	

Note 1: Tested but not recorded.

Note 2: Verified by functional testing

Mode Selection

Mode	CEB	OEB	WEB	PE	A(12:0)	I/O
Read	VIL	VIL	VIH	VIL	ADDR	DOUT
Standby	VIH	X	X	VIL	XXX	HIZ
Write	VIL	VIH	VIL	VIL	ADDR	DIN
Write Inhibit	X X	X VIL	VIH X	VIL VIL	XXX XXX	HI Z/DOUT HI Z/DOUT

Pin Description Addresses (A0-A12)

The address inputs select which byte will be accessed during a read or write operation. A0-A5 are the column or byte addresses and A6-A12 are the row or page addresses.

Chip Enable (CEB)

This input must be LOW during read and write operations. After a programming operation has been initiated, the chip may be deselected. When the part is deselected, the outputs are tristated.

Output Enable (OEB)

This input controls the output buffers. When HIGH the outputs are tristated and when LOW the outputs are driven to the correct CMOS levels.

Data (D0-D7)

Data is written to or read from the part using these pins.

Write Enable (WEB)

This input controls the writing of data. When low, write is enabled.

Clock Input (CLK)

The clock input is used to time the programming functions. The nominal value for a 10 ms write cycle is 2 MHz. The clock is not required for read operations. The clock waveform has no critical timing with respect to other input or output signals.

Reset Input (RSTB)

The reset input is active LOW and is used to prevent programming during power transitions or during high transient radiation doses. This signal should be held low during power up and power down.

Write Voltage (VW)

This -5V±5% supply pin is used to provide the internal programming voltage. This pin may be tied to OV during read operations. During power up VDD must come up first, then Vw; and during power down Vw must go off first, then VDD.

Charge Pump Enable (CPEB)

Must be tied to VDD. Reserved for future use.

Program Enable Input (PE)

This pin is used for testing and validation purposes to gain more control over internal chip operation. Normal operation requires this pin to be tied LOW. In READ ONLY (ROM) applications, this pin can be used to gain external control of the write timing to optimize retention. This feature is used when the device is programmed offline using a PROM programmer. The W28C64 is supported by the PROM programmer supplied by BP Microsystems, Houston, TX.

CAUTION: Device can be damaged if improperly programmed in external mode. For ROM applications, a PROM programmer is recommended. Contact Northrop Grumman for additional information. The optimized programming conditions used in the PROM programmer will result in longer retention, when frequent reprogramming is not a requirement. Under these conditions retention is specified as 100 years, at 80°C, with less than 200 programming cycles and less than 50 K Rads total dose.

Data Polling

The programming time for the W28C64 is controlled by an internal counter and the externally supplied clock input. The nominal timing is for a 10 ms programming time with a 2 MHz clock input. The Data Polling mode can be used to verify the completion of programming. If a read is performed on any address while the part is still being programmed, the ones complement of the last byte written will be presented at the outputs. After programming has completed, a read of the last address written will result in the correct data being presented at the outputs. To monitor for completion of programming the user can read the last address written until the correct data is read.

Data Retention

The W28C64 EEPROM is based on SONOS nonvolatile memory technology. SONOS is an acronym for Silicon-Oxide-Nitride-Oxide-Silicon. The memory device is a silicon gate N-channel MOS transistor with a specially processed gate dielectric consisting of a tunnelling oxide, a silicon nitride layer, and a capping oxide. SONOS technology is used in preference to conventional floating gate technology because of its superior reliability and radiation hardness.

The SONOS memory effect relies on charge storage within the silicon nitride film, with the silicon dioxide above and below it acting as energy barriers to the loss of charge. The charge is injected by tunnelling through the tunnelling oxide.

The charge deposited in the SONOS dielectric does decay slowly with time, but when written under the specified conditions and stored within the specified limits, data is indeed permanent for most purposes. Data loss is accelerated by both temperature and radiation, and is also affected by the number of write cycles the device has seen previously.

Write cycles must, however, be accumulated in the tens of thousands before any effect on retention is seen. When written using a 2 MHz external clock, nonvolatile data storage guaranteed through 100 K Rad (Si), without rewriting, at the specified temperature range. In satellite applications, this normally corresponds to many years of service.

For operation beyond 100 K Rad (Si), data should be written after every 100 K Rad of accumulated total dose. In addition to the memory devices themselves, a key feature of this device is the radiation hardened peripheral circuitry. This circuitry remains virtually unaffected by radiation effects within the limits specified over the full range of device operation.

For proper retention and reliability, the memory devices require careful control of the clear/write conditions. This applies particularly to the control of the clear/write voltage. The clear/write time (pulsewidth) is also important.

Consequently, both a Clock pin and a Vwrite pin are provided. With a nominal 2 MHz clock and Vw = -5V±5%, this device emulates commercial EEPROMs. Under these conditions, data retention is guaranteed for a minimum of 10 years. The external clock is required for write mode only, read mode is asynchronous and no clock is required.

Temperature	Retention (Years)	Cycles	Total Dose K Rad (Si)
-55 to 80°C	10	10,000	0 to 50
-55 to 80°C	10*	1,000	50 to 100

Rewriting after 100 K Rads results in another 10 years of retention up to a max total dose specified

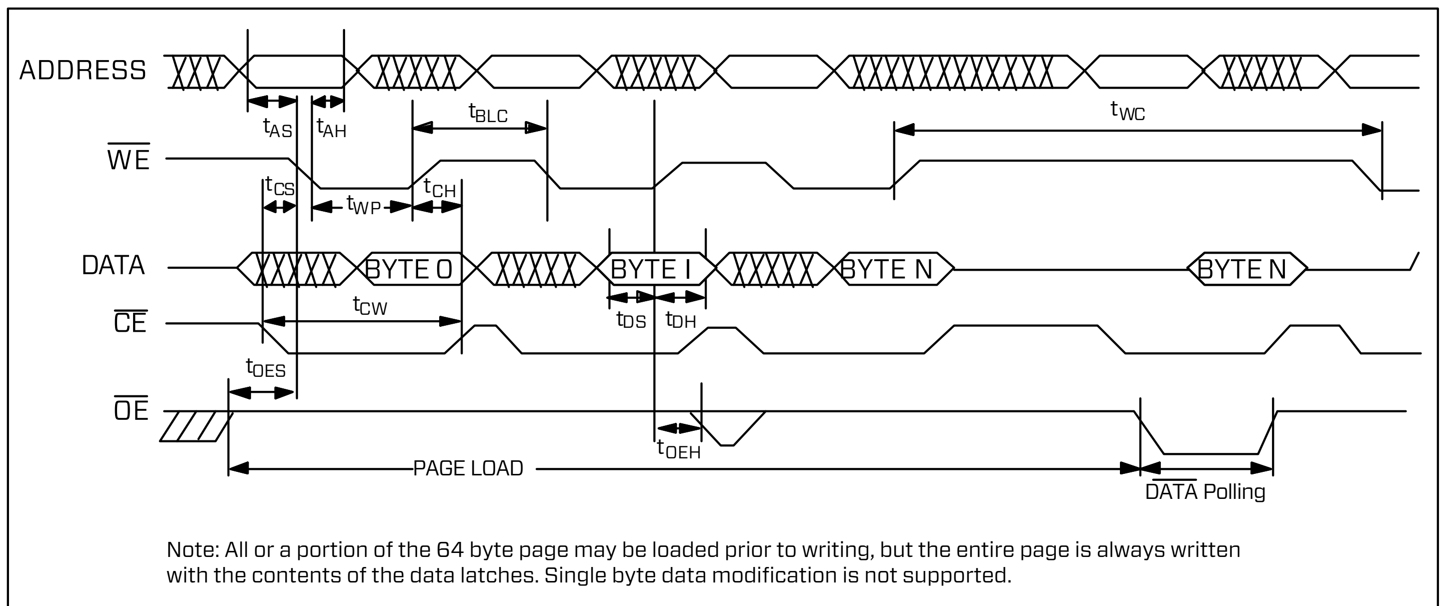
AC Operating Characteristics (Write Operations)

Guaranteed by design but not tested
Recommended Operating Conditions: T_A = -55 to +125°C, VDD = 5V ± 5%, unless otherwise specified

Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
^{t}C	Clock Frequency	1	2	MHz	Write Mode (Note 1)
^{t}WC	Write Cycle Time		10	ms	fc = 2 MHz (Note 1)
^{t}AS	Address Setup time	0		ns	
^{t}AH	Address Hold Time	150		ns	
^{t}CS	Write Setup Time	0		ns	
^{t}CH	Write Hold Time	0		ns	
^{t}CW	CEB Pulse Width	150		ns	
^{t}OES	OEB High Setup Time	10		ns	
^{t}OEH	OEB High Hold Time	10		ns	
^{t}WP	WEB Pulse Width	150		ns	
^{t}DS	Data Setup Time	0		ns	
^{t}DH	Data Hold Time	60		ns	
^{t}BLC	Byte Load Cycle	0.2	250	^{x}s	fc = 2 MHz

Note 1: Verified by functional testing.

Write Cycle



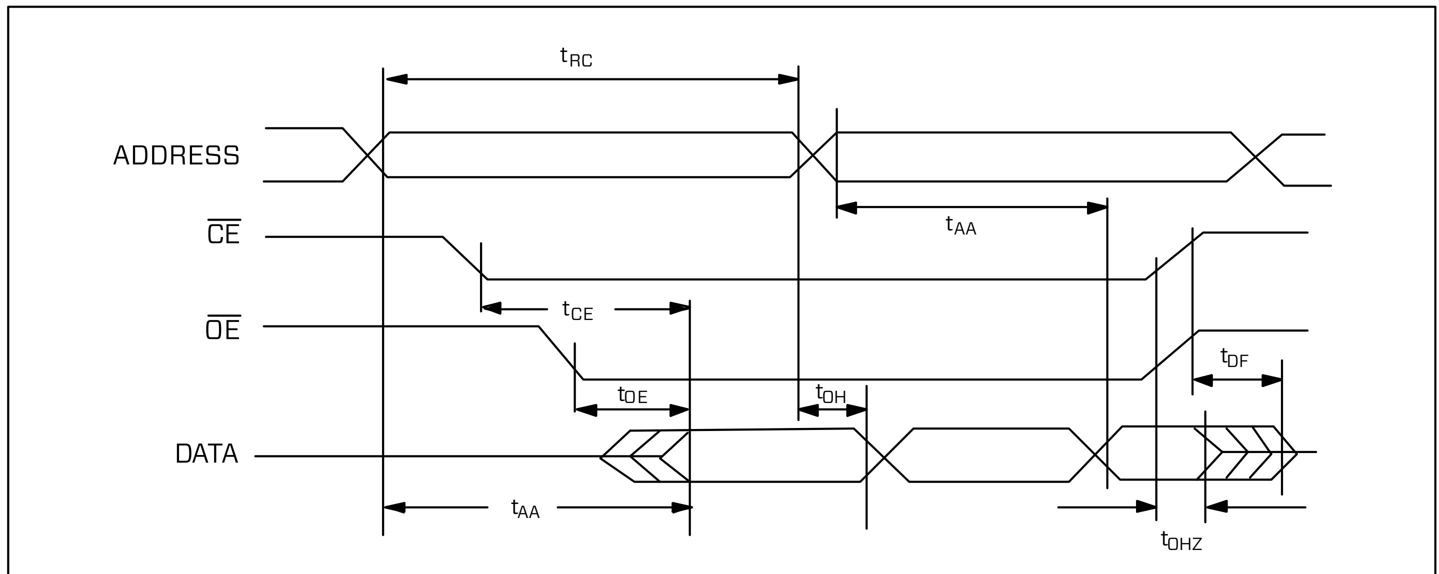
AC Operating Characteristics (Read Operations)

Guaranteed by design but not tested
Recommended Operating Conditions: T_A = -55 to +125°C, VDD = 5V ± 5%, unless otherwise specified

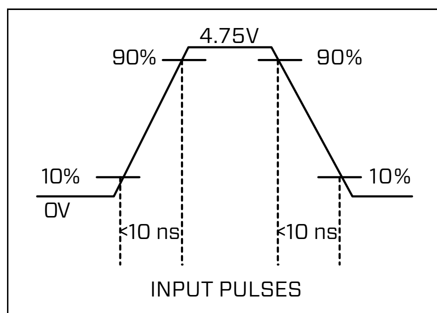
Symbol	Parameter	Limits		Units	Test Conditions
		Min	Max		
tRC	Read Cycle Time	250		MHz	
tCE	CEB Access time		250	ns	OEB = VIL
tAA	Address Access Time		200	ns	CEB = OEB = VIL
tOE	OEB Access Time		90	ns	CEB = VIL
tDF	OEB or CEB High to Output Hi Z		130	ns	CEB OR OEB = VIL IO = ±3mA
tOH	Output Hold from Address Change	0		ns	CEB OR OEB = VIL (Note 1)
tOHZ	OEB High to High Z Output	25		ns	IO = ±3mA

Note 1: Guaranteed but not tested.

Read Cycle



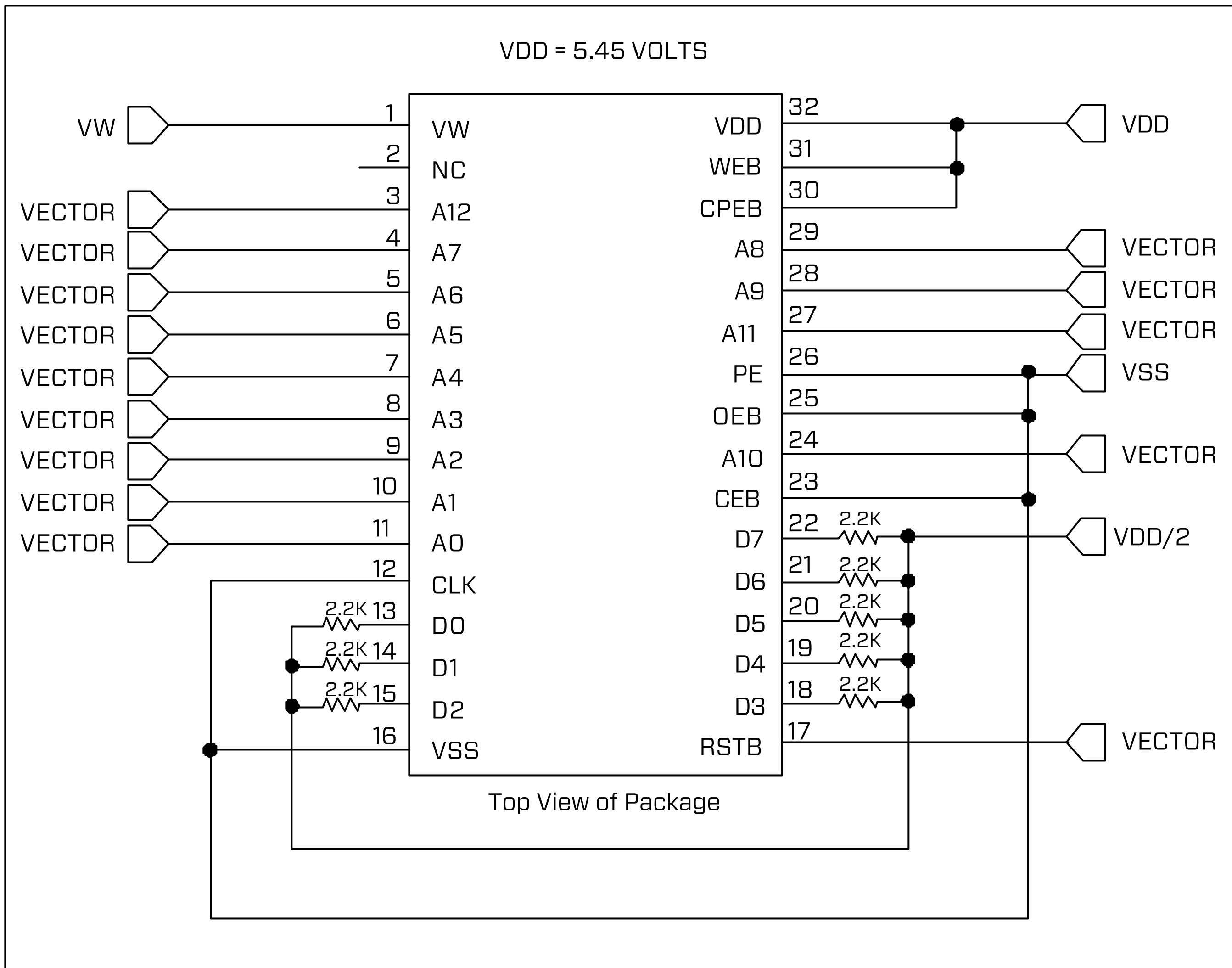
AC Test Loads and Input Waveforms



CAPACITANCE T_A = 25ºC f = 1 MHz

Symbol	Parameter	MAX	Conditions
C_{IN}	Input Capacitance	5pF	Vin = 0
C_{OUT}	External Load Capacitance	70pF	AC Operations

Dynamic Burn-In Circuit

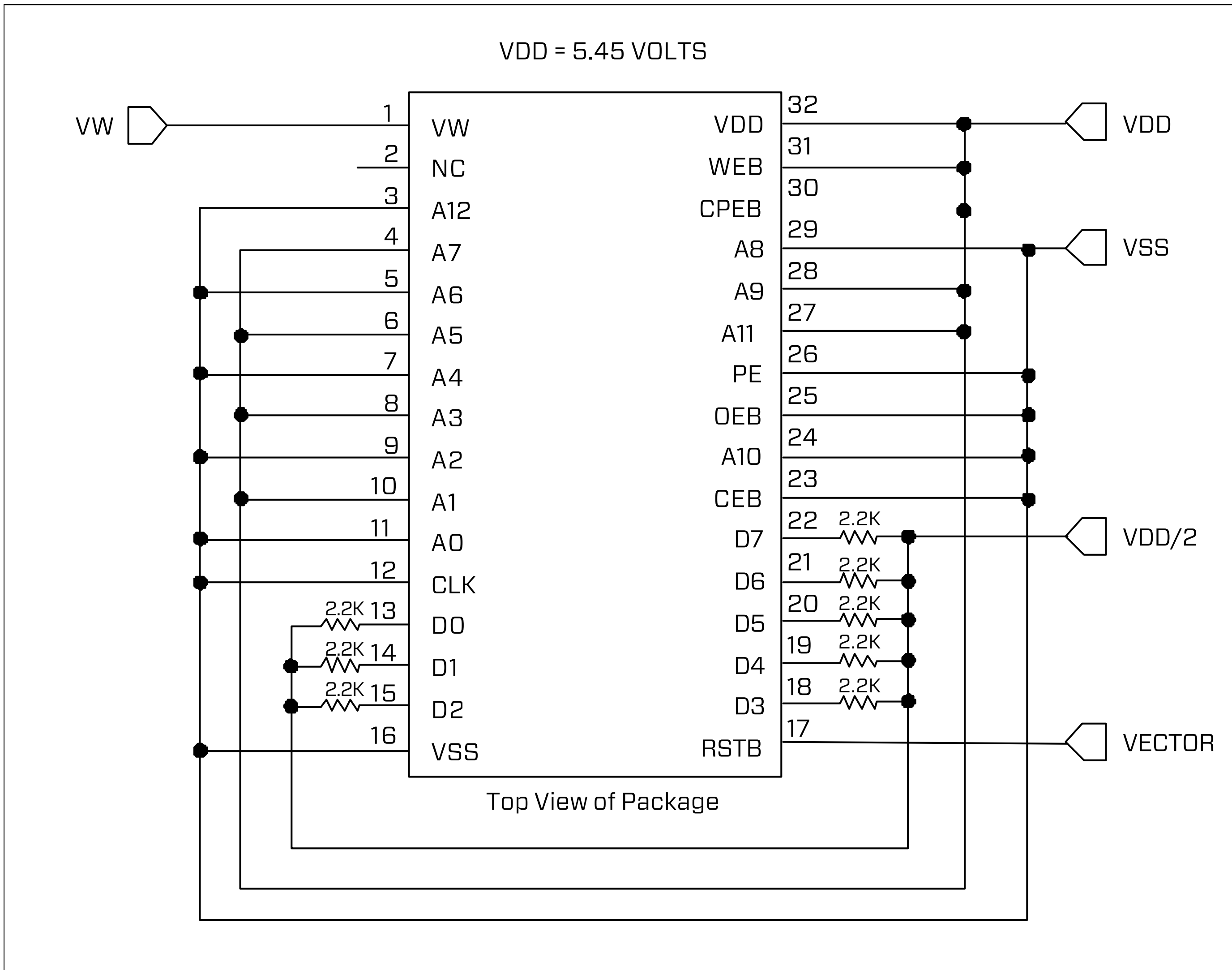


Note 1: Incorporate isolation resistors (~3K ohm) at inputs labeled "vector"; i.e., pins 3-11, 17, 24 and 27-29. (Total of 14 resistors/device location).

Note 2: For Dynamic Burn-in

VW	=	GND
RSTB	=	GND
CPEB	=	HIGH

Static Burn-In Circuit



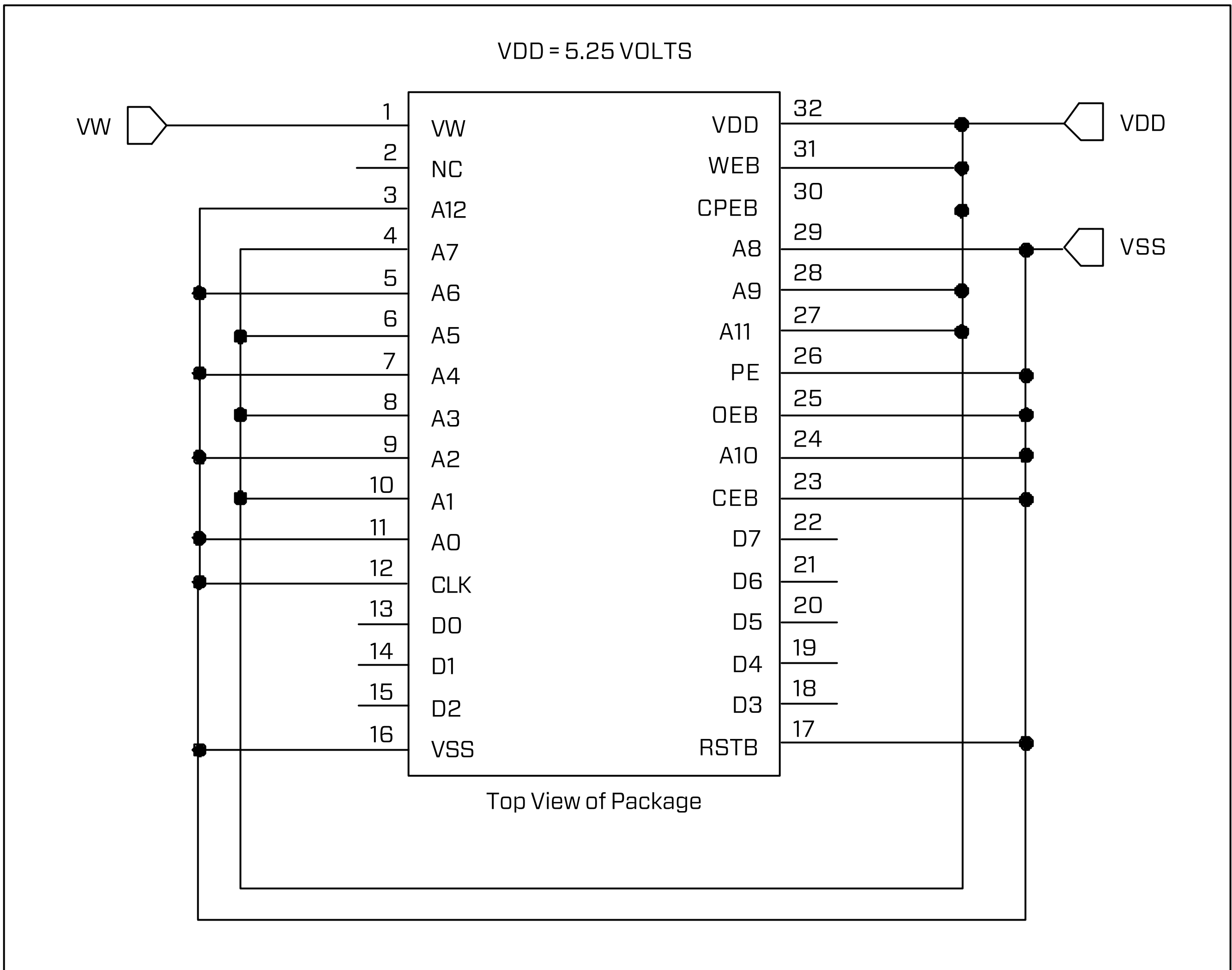
Note 1: Incorporate isolation resistors (~3K ohm) at pins 3-11, 17, 24 and 27-29.
(Total of 14 resistors/device location).

Note 2: VW = GND

Note 3: CPEB = HIGH

Note 4: RSTB = GND

Radiation Bias Circuit

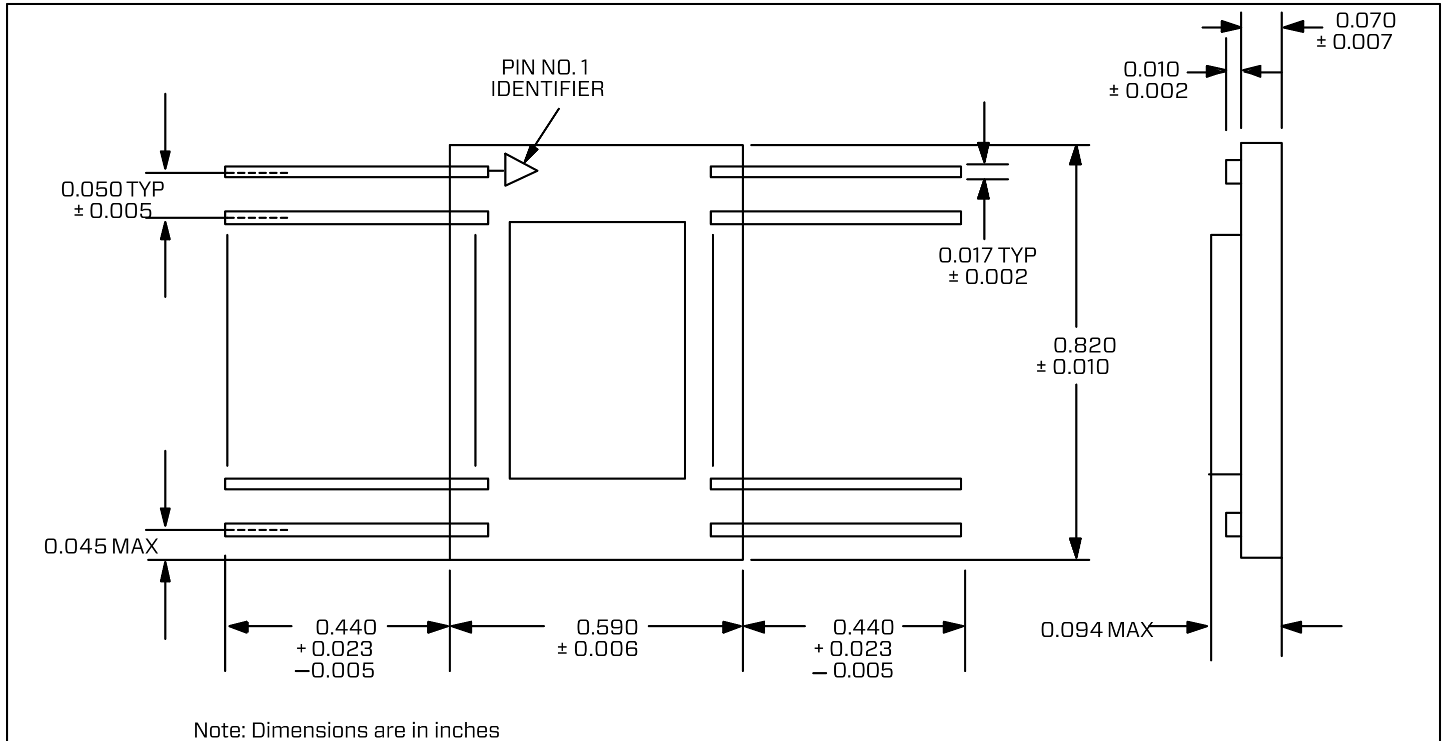


Note 1: VW = GND

W28C64 Die Information

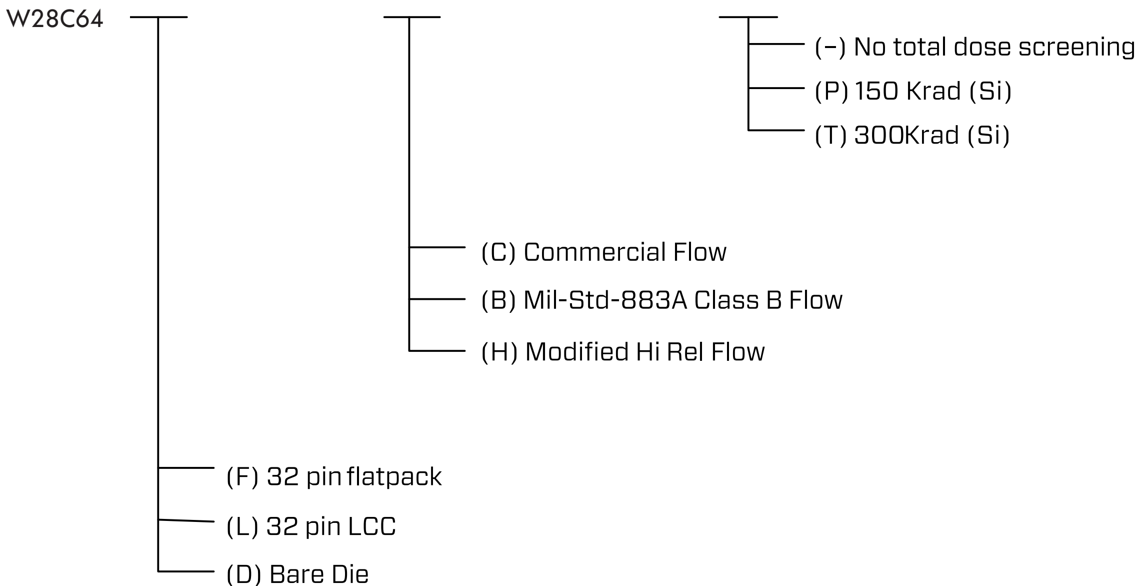
32 Pin Ceramic LCC Package

32 Pin Flatpack



Ordering Information

To order the W28C64 radiation hardened EEPROM, use the following part numbers.



Distribution is Unlimited; #21-0465; Dated 03/17/21
Specifications and features subject to change without notice.
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